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THESIS

DESIGN, CONSTRUCTION, AND TESTING OF A HYSTERESIS CONTROLLED INVERTER FOR PARALLELING

by

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September 2003

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The U. S. Navy is pursuing an all electric ship that will require enormous amounts of power for applications such as electric propulsion. Reliability and redundancy in the electronics are imperative, since failure of a critical system could leave a ship stranded and vulnerable. A parallel inverter drive topology has been proposed to provide reliability and redundancy through load sharing. The parallel architecture enables some functionality in the event that one of the inverters fails. This thesis explores paralleling current-mode inverters of different power levels and fidelities. A 50-kVA, three-phase hysteresis controlled inverter is designed, built, and tested at low power. The inverter is then tested in parallel with a low frequency, bulk inverter to demonstrate current sharing capability.

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DESIGN, CONSTRUCTION, AND TESTING OF A HYSTERESIS CONTROLLED INVERTER FOR PARALLELING

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ABSTRACT

The U. S. Navy is pursuing an all electric ship that will require enormous amounts of power for applications such as electric propulsion. Reliability and redundancy in the electronics are imperative, since failure of a critical system could leave a ship stranded and vulnerable. A parallel inverter drive topology has been proposed to provide reliability and redundancy through load sharing. The parallel architecture enables some functionality in the event that one of the inverters fails. This thesis explores paralleling current-mode inverters of different power levels and fidelities. A 50-kVA, three-phase hysteresis controlled inverter is designed, built, and tested at low power. The inverter is then tested in parallel with a low frequency, bulk inverter to demonstrate current sharing capability.

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EXECUTIVE SUMMARY

Today's Naval ships require enormous amounts of electric power to operate a variety of equipment including a seaman's electric razor, sophisticated radars and computers, and high power motors. As progress is made toward an "all electric ship", the ability to distribute and control power to various loads becomes increasingly critical.

Generators aboard ship churn out electricity, which may undergo several transformations before powering a particular load. Controlling ac power to a motor load normally involves converting the ac source into dc, then into ac appropriate for the load, i.e., at the correct magnitude and frequency. An electronic circuit that converts dc into ac is called an inverter. In general, two types of inverters exist: Voltage Source Inverters (VSI) and Current Source Inverters (CSI). Current source inverters are normally used in high power ac motor drives and are the basis for this thesis.

Inverters have been and will continue to be an indispensable part of power electronics aboard Naval ships well into the future. For example, the U. S. Navy is currently pursuing Electric Propulsion Drive Systems (EPDS) using electric propulsion motors with a rated power of 38 MW. EPDS will require advanced inverter technology to provide reliability and adequate power. Paralleling inverters has been proposed to offer both reliability through redundancy and high power through current sharing. If only one inverter drive was used for such an application, failure could leave a warship stranded and vulnerable. Thus, redundancy in inverter drives is of critical importance. Additionally, connecting two or more identical inverters in parallel provides two or more times the current capacity of a single inverter drive [1,2].

This thesis examines a 50-kVA, three-phase CSI, with a hysteresis controller. The goals are to design, build, and test an inverter that can be operated in parallel with a number of other inverters. Hysteresis control is not a new idea and publications describing its theory and application are readily available [3,4,5]. However, its use in high power inverter modules or in paralleling inverters is not as well publicized. In fact, the development of high power inverter modules, in general, is in its infancy [2]. Therefore, a study of parallelable hysteresis controlled inverters that could be used to improve the

output waveform of a high power bulk inverter (such as a 6-step) is warranted. This thesis presents the design, computer simulation, building, and testing of a single inverter. To test the inverter for parallel operation, a square-wave signal was injected into the load to simulate the input of a parallel bulk inverter. Test results are provided in Chapter V of this thesis.

I. INTRODUCTION

The goal of this thesis is to demonstrate the viability of parallel inverter topology for high power applications. This chapter presents the applicability of this work to current U. S. Navy research interests and gives a synopsis of following chapters.

A. BACKGROUND AND MOTIVATION

As the U. S. Navy makes progress toward an "all electric ship", various new technologies are explored and studied. The Office of Naval Research (ONR) has begun the Advanced Electrical Power Systems (AEPS) program to study electrical power distribution aboard ships. One of the goals of this program is to increase power density by reducing the size, weight, and cost of the electronics. Another goal is to reduce the need for custom circuitry in favor of modules capable of performing a variety of functions via initial programming. The concept is to develop a set of generic power modules capable of converting one flavor of power to another that is load specific. Such a module would contain input and output power terminals and a programmable port for defining the module's use, i.e. dc–ac, ac–dc, dc–dc, ac–ac, etc. More information about the AEPS program can be found at the ONR website: www.onr.navy.mil.

With these goals in mind, the concept of paralleling generic inverter modules holds promise for use on future ships to control high power ac motors. Multiple inverters operating in series/parallel allows for load sharing. Thus, a single modular type of inverter could be used for every shipboard application requiring inverters. Those that require higher power would simply have the appropriate number of inverters wired in parallel and/or series to account for the voltage and current. Additionally, paralleling inverters provides reliability through redundancy. However, this technology is not yet mature enough for shipboard applications [1,2].

The aim of this thesis is to theoretically and experimentally analyze hysteresis control for use in parallel Current Source Inverters (CSI). To that end, such a controller was designed and assembled in an existing 50-kVA power section of a water-cooled, three-phase inverter. The inverter was tested as a stand-alone unit then evaluated for possible parallel operation with another inverter.

B. APPROACH

The existing inverter had an overly-sophisticated Digital Signal Processing (DSP) controller that was not necessary for the work performed in this thesis. The DSP control circuitry was replaced with an appropriate controller that could be built with readily available components. A hysteresis controller was chosen as the replacement because it allows for easy paralleling with inherent short-circuit protection.

The control circuitry was first designed and assembled on a proto-board, then tested to verify that the approach and design had merit. Next, a computer simulation was done to determine the relationship between switching frequency, load inductance, load resistance, and voltage levels (dc link and output). Then, a three-phase controller board was fabricated and assembled using wire-wrap and copper sheeting. The board was mounted and wired to the inverter and tested.

Finally, an experiment in paralleling two inverters was performed. To accomplish this testing, a square wave signal was injected into the load current and the inverter response was analyzed.

C. THESIS ORGANIZATION

Chapter II is an introduction to CSIs and will serve as a refresher on some inverter basics. This chapter quickly progresses from the most basic concepts to sine-Pulse-Width-Modulation (PWM). Some of the limitations of rudimentary control techniques are addressed.

Chapter III presents hysteresis control. The basics of hysteresis control are discussed concurrently with the fabrication of the controller.

Chapter IV discusses component parameters and limitations, and the MatLab computer simulation. While designing and building the inverter, the tolerances and characteristics of the chosen components must be understood to ensure they are appropriate for this application. Certain limitations, such as maximum switching frequency and circuit delays, are considered in the design. The design was simulated in MatLab, which provides basic parameters for testing the circuit at low current. A simulation was also

done to show operation at rated power. Additionally, a comparison between different switching schemes was performed through simulation.

Chapter V is the presentation of experimental results. The inverter was tested as a stand-alone unit at low current to verify the results of the simulation. An experiment in parallel operation was also performed.

Chapter VI contains the conclusions. Recommendations are made to enhance the controller and a proposal for follow-on work is included.

Appendices A and B are the MatLab code written to simulate the inverter. Appendix C contains wiring and pin diagrams for the various components of the inverter.

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II. BASICS OF CURRENT SOURCE INVERTERS

An inverter, quite simply, converts dc power from a dc source to ac at a desired frequency, voltage, and current. A CSI is specifically designed to produce an ac current and is fed from a dc voltage source. The dc power is usually derived from some form of rectification or battery source. Typical applications of inverters include inductive heating, standby power supplies, and ac motors. Aboard ships, typical applications include induction motors in pumps, compressors, or fans. This chapter is an introduction to CSIs and traditional control strategies.

A. SWITCH MODE INVERTERS

Converting dc to ac is often accomplished using switch-mode inverters. A simple single-phase inverter called a half-bridge is shown in Figure 1. An ac source is converted to dc via a full-wave diode bridge rectifier with a two-pole filter (L_f and C_f). The capacitors C_1 and C_2 provide a virtual midpoint between the "upper rail" voltage, V^+, and the "lower rail" voltage, V^-. In other words, C_1 and C_2 block the dc component so that the *RL* load sees only ac. Switches S_1 and S_2 are opened and closed at a desired frequency to produce an alternating current through the inductive load. Note that both switches are should never be closed at the same time. The diodes (D_1 and D_2) across the switches are necessary to provide a path for the current after the opposite switch turns off. The current through the inductor at any time, *t*, is governed by the equation

$$i(t) = i(t_0) + \frac{1}{L}\int_{t_0}^{t} v_L(\lambda)d\lambda \qquad t > t_0, \tag{2.1}$$

where $i(t_0)$ is the initial current, v_L is the voltage across the inductor, and *L* is the inductor value.

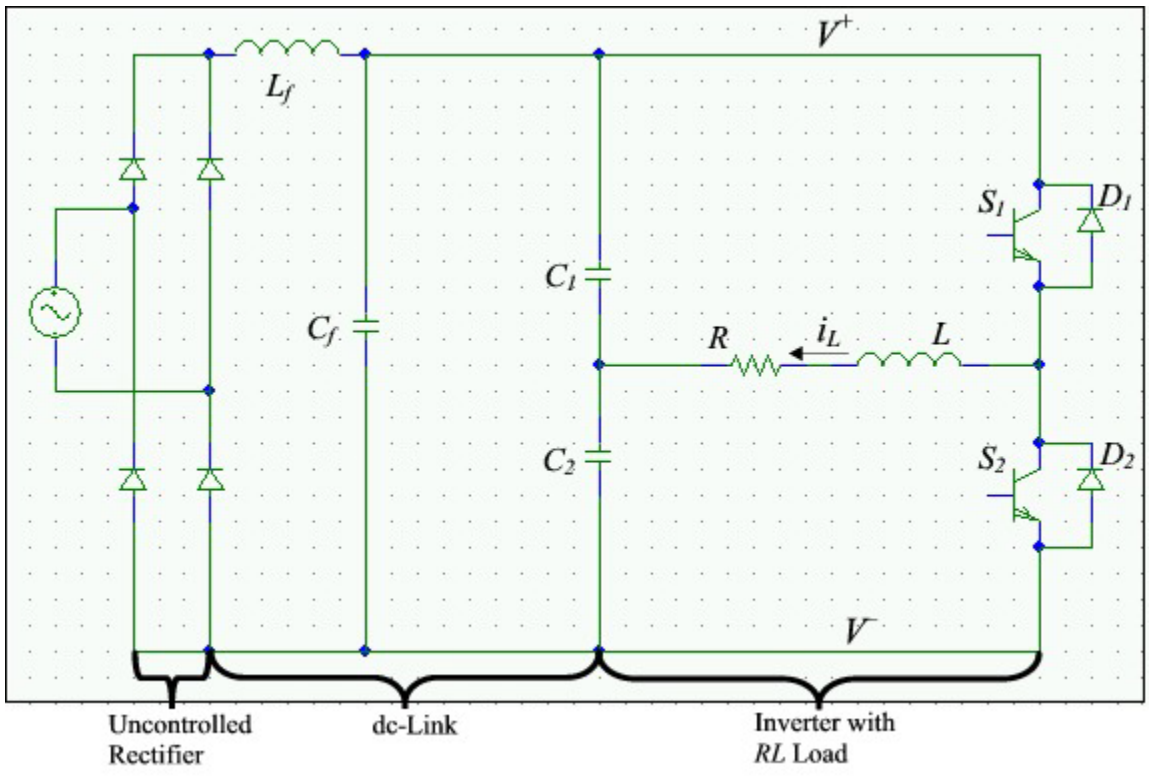

Figure 1. Representation of One Half-Bridge of the Three-Phase Inverter.

To produce a 60-Hz alternating current, the switches could be turned on and off at a constant 60-Hz frequency. This method requires no feedback or monitoring of the load current and is very simple to implement. Such a switching pattern would produce the load current shown in Figure 2. The upper waveform in Figure 2 is the load current and the lower waveform is the voltage across the *RL* load. Although the current waveform is clearly that of an alternating current, it does not closely resemble a sinusoid. The desire is to produce a current waveform that is as close to sinusoidal as possible. A good sinusoidal waveform is necessary to avoid torque pulsations for smooth and efficient operation of a traditionally sinusoidally wound induction motor. Additionally, this simple switching scheme only allows limited control of the output. The magnitude could be adjusted by varying the dc-link voltage with a more complicated converter. A higher or lower frequency is easily obtainable by simply increasing or decreasing the switching frequency, but neither of these adjustments will enhance the load current waveform. A more advanced switching method is needed and is presented in the next section.

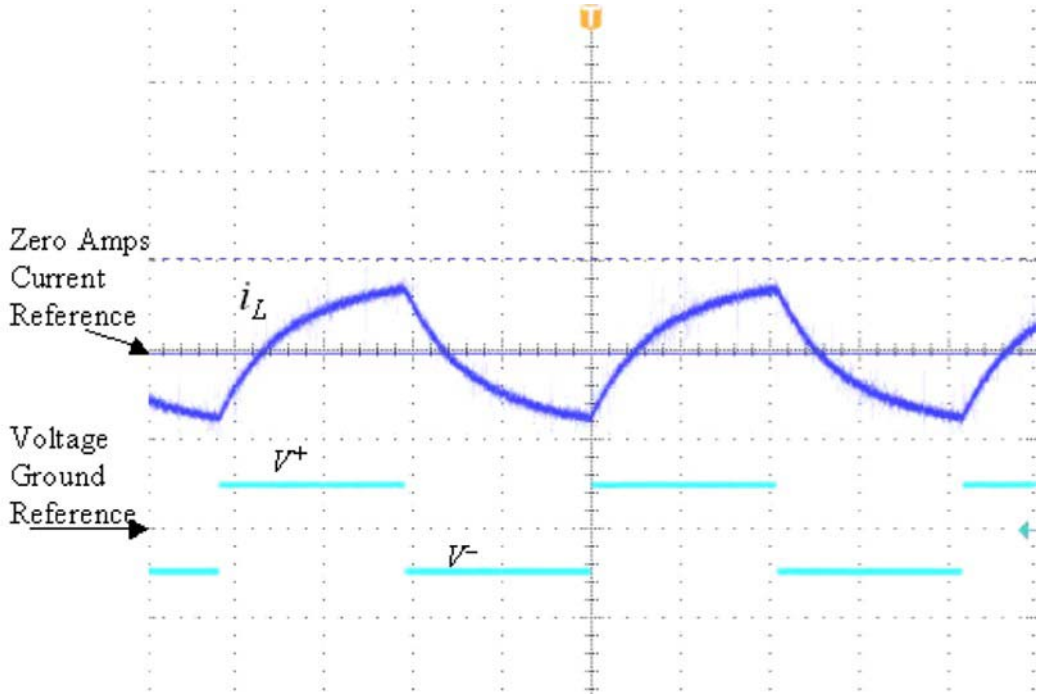

Figure 2. Basic Half-Bridge Waveforms for (Top) Load Current and (Bottom) Load Voltage.

B. TRADITIONAL CONTROL STRATEGY

Traditionally, inverters are controlled by a PWM strategy. PWM involves turning the switches on and off multiple times per half cycle to produce a periodic symmetrical waveform. This control method is well studied and publications of advanced PWM techniques abound. One particular and popular PWM strategy is called sine-PWM, in which a triangle wave is modulated by a lower frequency sine wave to produce the transistor gating signals (the signals which turn the transistor "on" or "off"). Figure 3 shows a graphical representation of this technique. Generally, harmonics are minimized by locking the frequencies of the sine and triangle waves such that odd integer numbers of gating pulses are produced per half cycle. If a system is polyphase, harmonic reduction can be further improved by choosing odd multiples of the phase count. For instance, a three-phase system would have the best reduction using odd triplets per half cycle (3, 9, 15, 21, etc.), where higher pulse count is preferred. Pulse count is limited by switching losses and therefore must be optimized for every inverter. It should be noted that, if the pulse

count per half cycle is greater than 100, there is negligible benefit to the above technique. However, for high power military inverters, this is rarely the case.

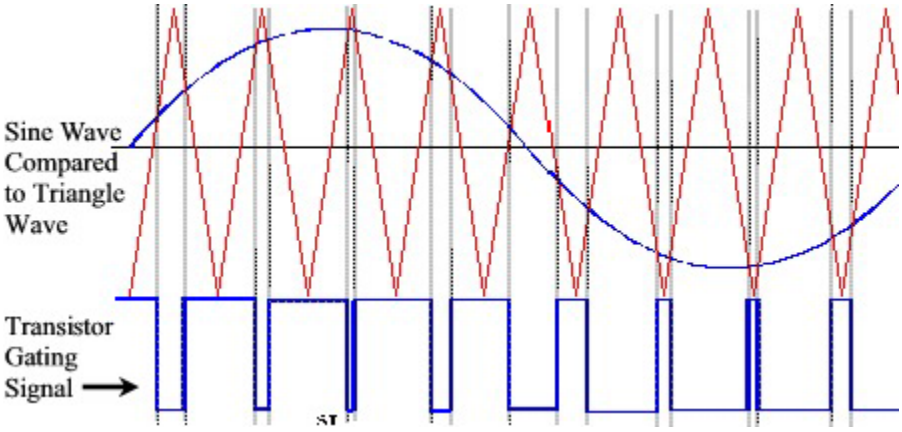

Figure 3. Sine-PWM and Gating Signal [After Ref. 6.].

Figure 4 shows a simple circuit to produce the gating signal. No feedback or monitoring of the load current is required. The magnitude of the load current is controlled by adjusting the voltage in the dc link or the magnitude of the sine wave with respect to the triangle wave. The frequency of the load current can also be adjusted by changing the frequency of the modulating signal. Figure 5 is an example of the load current waveform produced by sine-PWM, which is a more sinusoidal than the one shown in Figure 2.

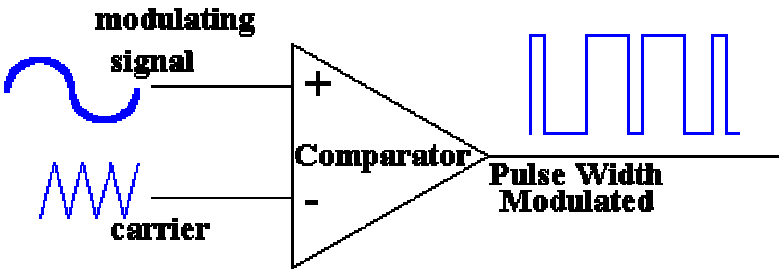

Figure 4. Simple Sine-PWM Circuit [From Ref. 6.].

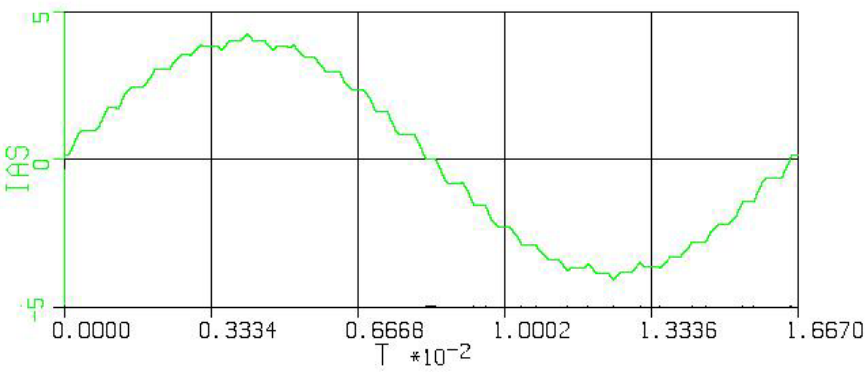

Figure 5. Load Current Waveform Produced by Sine-PWM [From Ref. 7.].

C. SUMMARY

Converting dc to ac is not difficult and can be accomplished using simple, inexpensive Commercial Off-The-Shelf (COTS) components. One method for controlling the output is sine-PWM, which can yield an acceptable sinusoidal load current for most applications. Although all the examples in this chapter were of single-phase inverters, the extension to polyphase systems is straight-forward and can be accomplished by applying the single-phase principles to each phase. The next chapter introduces another method called hysteresis control.

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III. HYSTERESIS CONTROL

The control methods presented thus far have been possible without any type of feedback. Hysteresis control requires feedback of the output current. This chapter describes in detail how hysteresis control can be implemented for a single-phase inverter.

A. CONCEPT OF HYSTERESIS CONTROL

Hysteresis control (also called "bang–bang" or "tolerance band" control) utilizes a defined upper and lower limit based on a reference waveform. The load current is monitored and maintained within certain limits of that reference waveform [8,9].

1. The Hysteresis Band

The hysteresis band defines an acceptable error in the load current based around a reference ac waveform, i_{ref}. By simply applying a positive and negative dc offset, I_h, to i_{ref}, the hysteresis band, Δ_h, is established [10]. More precisely, Δ_h is defined as the difference between the upper and lower boundaries,

$$\Delta_h = i_{\text{ref}} + I_h - (i_{\text{ref}} - I_h) = 2I_h. \tag{3.1}$$

A hysteresis control circuit monitors the load current and appropriately switches the transistors to ensure the load current remains within the hysteresis band. In the control circuit, i_{ref} is represented as a voltage proportional to the desired output current, i_{out}, with a conversion factor of 1 A/V. (In fact, all currents are converted to voltage signals at 1 A/V for ease of use by the control circuit.) Figure 6 shows a 2-A_{peak}, 60-Hz waveform, i_{ref}, with $I_h = 0.2$ A ($\Delta_h = 0.4$ A). The hysteresis band in Figure 6 appears wider at the upper and lower peaks than at the zero crossing; however, the band is measured vertically at a specific time instant and is a constant 0.4 A throughout the cycle.

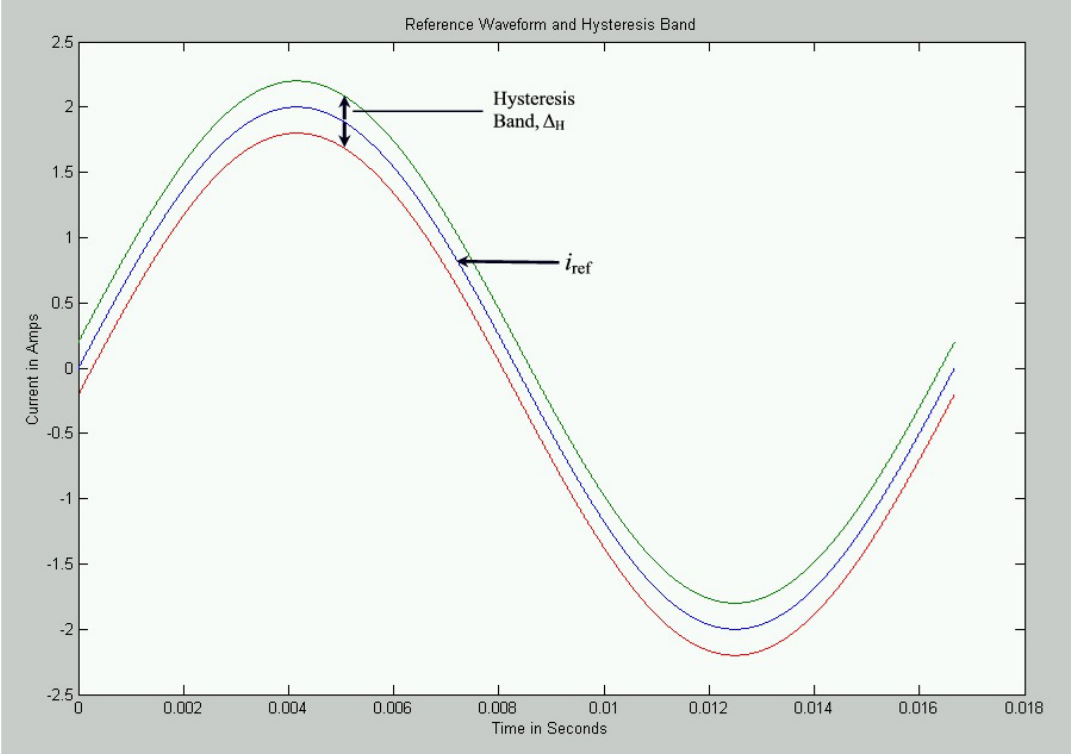

Figure 6. Hysteresis Band.

The circuitry required to define the hysteresis band uses summing and difference amplifiers, as shown in Figure 7. This circuit is a modification of one developed by the University of Missouri-Rolla [11].

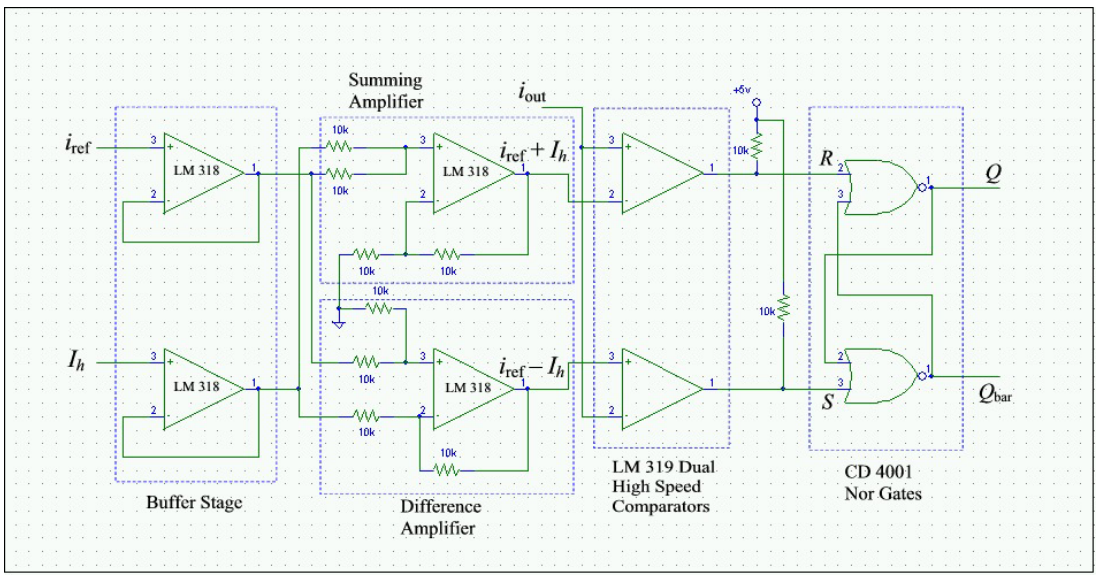

Figure 7. Hysteresis Control Circuit.

2. Feedback

Measurement of the load current is accomplished via a Hall effect device, which provides electrical isolation between the load current and control electronics [8]. A Hall effect device senses the load current and produces its own output current proportional to the load current. The current from the Hall effect sensor is passed through a measuring (burdening) resistor to produce a voltage that corresponds to the measured current. Thus, by appropriate choice of the measuring resistor, the feedback signal can be scaled making it possible to monitor and control a very large load current with a small feedback signal, i_{out}.

As shown in Figure 7, i_{out} is fed into a pair of comparators to determine whether or not it has reached one of the boundaries of the hysteresis band. When i_{out} reaches a boundary, the comparators force the *RS* flip-flop to change state and switch the transistors "on" or "off" as appropriate.

3. Gating Signals

Gating a transistor means turning it "on" and should not be confused with the digital logic term "gate", as in "nor gate". The *RS* flip-flop provides the gating signals for the transistors. Figure 7 shows the *RS* flip-flop implemented with two "nor" gates and Table 1 contains the function table for an *RS* flip-flop. Even though the flip-flop has the indeterminate state $R = S = 1,$ this state is impossible; the only way that $R = S = 1$ can occur is if the measured feedback signal, $i_{\text{out}},$ is both above and below the hysteresis band at the same instant in time. Should the flip-flop, for some reason, be in the indeterminate state at start-up, the control circuitry will immediately force it to exit that state and go to one of the other three states. The output of the flip-flop is used to gate the transistors; Q gates the upper and Q_{bar} gates the lower.

R	*S*	*Q*	Q_{bar}
0	0	No Change	
0	1	1	0
1	0	0	1
1	1	Indeterminate	

Table 1. *RS* Flip Flop Function Table.

B. SUMMARY

Hysteresis control is an alternative to the methods previously presented. Using feedback to monitor the load current, the control circuitry will cause the load current to follow a reference waveform.

In the next chapter, the components used to construct a working inverter are examined. Values for load inductance, resistance, and switching frequency are discussed with the help of a MatLab program.

IV. DESIGN PARAMETERS

This chapter presents the integration of the hysteresis controller into a working inverter. The individual components of the inverter are analyzed and their voltage, current, and maximum ratings are used to properly design the inverter controls. A MatLab simulation provides analysis of the design and displays the load current as it follows the reference.

Figure 8 shows a schematic of the power section of the three-phase inverter. Each phase has a Hall effect device to measure the current and provide feedback to the hysteresis controller. The controller operates each phase independent of the others, so much of the analysis and simulation in this chapter will be performed for the single-phase case.

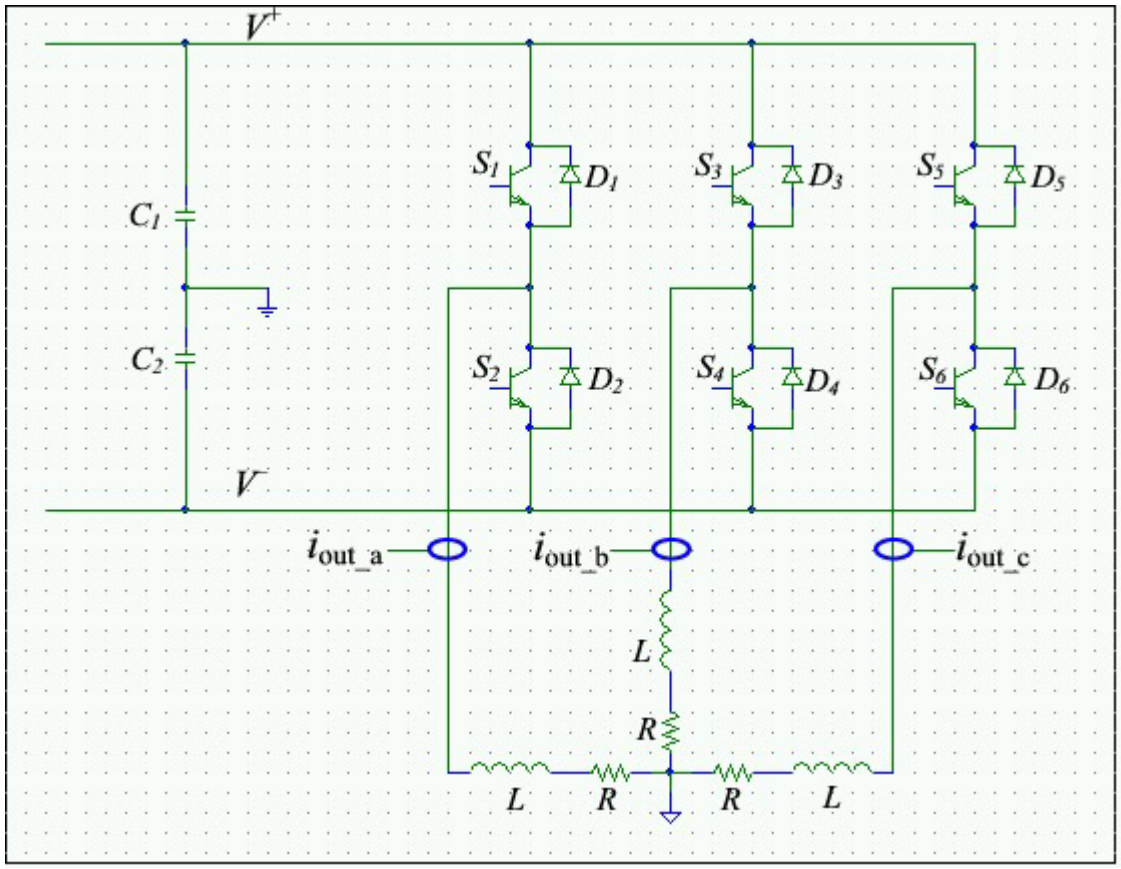

Figure 8. Power Section of the Three-Phase Inverter.

A. COMPONENTS

The inverter has many components. The most notable power components are the dual Insulated Gate Bipolar Transistor (IGBT) modules, dual IGBT drivers, and current transducers (Hall effect devices). A review of the data sheets for the chosen IGBTs and drivers revealed that they are rated at a collector current $I_c = 200$ A and a collector-to-emitter voltage $V_{ce} = 1200$ V. Given the enormous differences between the magnitudes of the control and power voltages and currents, electrical isolation was deemed necessary. Good quality drivers provide galvanic isolation, as well as short-circuit protection by V_{ce} monitoring and shutdown. Additionally, many drivers include circuitry to ensure minimum transistor on-times and off-times are met.

1. Dual Insulated Gate Bipolar Transistors (IGBT) Modules

The IGBT modules are Powerex CM200DY-24H. Each module contains two IGBTs in a half-bridge configuration. The manufacturer's recommended switching frequency is $f_s = 20 - 25$ kHz. However, the inverter will operate at a variable switching frequency, so the maximum allowable switching frequency, f_{max}, of the IGBTs must be calculated. A critically important characteristic is the minimum allowable on-time, $t_{on(min)}$, of the transistor, which must not be breached in order to avoid damaging the transistor. The data sheet does not specify the minimum on-time, but does list characteristics of the switching times, as shown in Table 2, where V_{cc} is the dc bus voltage (half-bridge configuration); I_c is the collector current; V_{ge1} and V_{ge2} are the gate-to-emitter voltages for transistors 1 and 2, respectively; and R_g is the gate resistance.

Characteristic	**Symbol**	**Max**	**Units**	**Test Conditions**
Turn-on Delay Time	$t_{\mathrm{d(on)}}$	250	ns	$V_{\mathrm{cc}} = 600$ V, $I_c = 200$ A, $V_{ge1} = V_{ge2} = 15$ V, $R_g = 1.6\ \Omega$.
Rise Time	t_r	400	ns	
Turn-off Delay Time	$t_{\mathrm{d(off)}}$	300	ns	
Fall Time	t_f	350	ns	

Table 2. IGBT Switching Characteristics.

These switching characteristics are displayed in Figure 9, which plots V_{ce} against time (ns) for one switching cycle. Although a minimum conduction time is not specified in the data sheet, a safe estimate, excluding any turn-off delay time, can be calculated. This is accomplished by assuming that the minimum conduction time, $t_{\mathrm{on(min)}}$, and minimum off time, $t_{\mathrm{off(min)}}$, (excluding delay times) are defined by

$$t_{\mathrm{on(min)}} = t_{\mathrm{d(on)}} + t_r \tag{4.1}$$

and

$$t_{\mathrm{off(min)}} = t_{\mathrm{d(off)}} + t_f . \tag{4.2}$$

Substituting values from Table 2 yields $t_{\mathrm{on(min)}} = t_{\mathrm{off(min)}} = 650$ ns. Summing these times with those in Table 2 and taking the reciprocal gives $f_{\max} \approx 385$ kHz. However, this in no way can be sustained because of switching losses. Further, there are no COTS drivers that could approach this switching frequency. For instance, the Semikron drivers used for this application have a maximum switching frequency of 50 kHz.

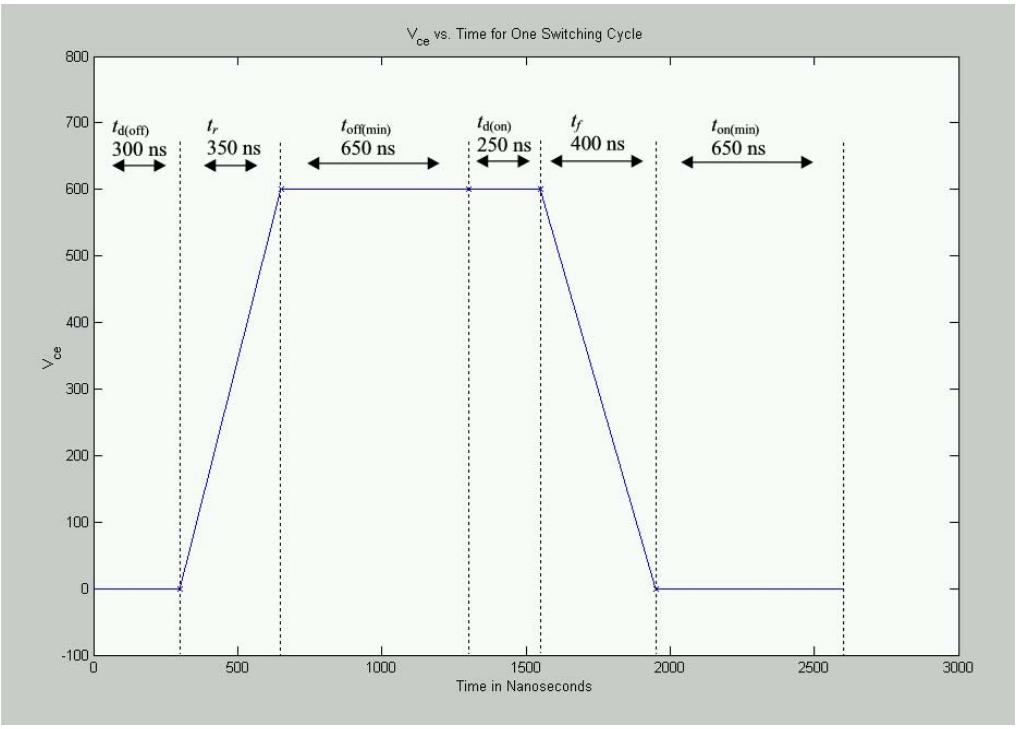

Figure 9. IGBT Switching Characteristics.

In addition to the switching characteristics of the IGBTs, power losses must also be examined. The IGBT modules are mounted on an aluminum, water-cooled heat sink, as shown in Figure 10.

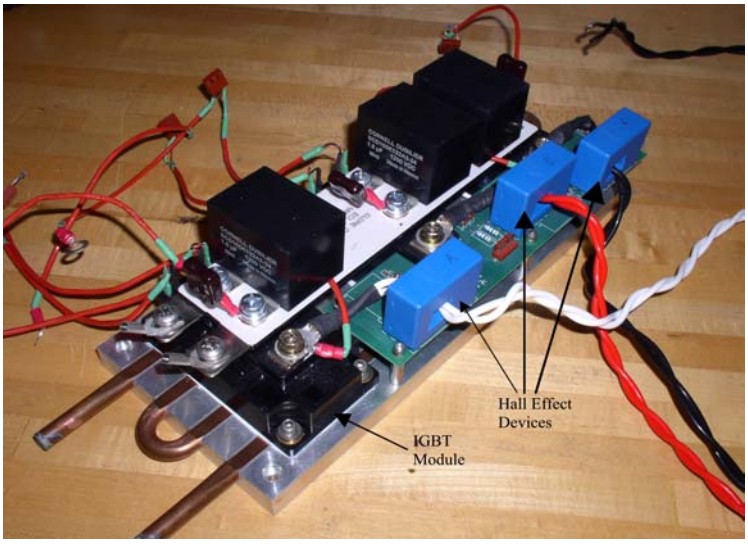

Figure 10. IGBTs with Hall Effect Devices.

While the specification sheet does not list power dissipation for such a heat sink, it does state that the modules can dissipate 1500 watts. The power losses can be broken into four parts: conduction losses, P_c; substrate diode conduction losses, P_{sd}; switching losses, P_s; and reverse recovery diode losses, P_{rr}. For the half-bridge configuration shown in Figure 8, it is imperative that substrate diode losses be considered. When switch S_1 opens and S_2 closes during the positive half-cycle of the load current, the current travels through the substrate diode D_2 rather than the switch itself. For the negative half-cycle, switching roles are reversed and the current will travel through the substrate diode D_1. All four power losses are estimated by the following equations:

$$P_c = V_{\text{ce(sat)}} I_c \frac{t_{\text{on}}}{T_s}, \tag{4.3}$$

$$P_{\text{sd}} = V_d I_c \frac{t_{\text{on}}}{T_s}, \tag{4.4}$$

$$P_s = 0.5 V_{\text{cc}} I_c \frac{1}{T_s}(t_r + t_f), \tag{4.5}$$

and

$$P_{\text{rr}} = 0.125 I_{\text{rr}} t_{\text{rr}} V_{\text{dr}} f_{\text{max}}, \tag{4.6}$$

where $V_{\text{ce(sat)}}$ is the collector-to-emitter saturation voltage, I_c is the collector current, t_{on} is the transistor on-time, T_s is the switching period, V_d is the voltage drop across the substrate diode, V_{cc} is the dc bus voltage (half-bridge configuration), t_r is the rise time, t_f is the fall time, I_{rr} is the diode peak reverse recovery current, t_{rr} is the diode reverse recovery time, V_{dr} is the peak voltage across the diode at recovery, and f_{max} is the maximum switching frequency [8,12,13]. Notice that P_s depends on the collector current. For cases when a switch turns "on" and "off", but the current travels through the substrate diode rather than the collector, there are no switching losses; such losses are diode reverse recovery losses. The total losses are given by

$$P_{\text{tot}} = P_c + P_{\text{sd}} + P_s + P_{\text{rr}}. \tag{4.7}$$

Because of the sinusoidal varying output waveform and the varying switching frequency, the number of individual calculations necessary to compute power losses is enormous. The only practical method of determining losses is through simulation and experimental verification. The power losses are calculated in a MatLab simulation of the inverter. The equations above give "worst case" estimations of the power losses, but yield good values for design considerations. For the initial testing of the inverter at low power, the total losses are less than 10 watts, so are deemed negligible. However, the losses are an important factor at full power. Losses at full power are presented later in this chapter in a Section C.

2. Dual IGBT Drivers

The drivers are Semikron's SKHI 21B Hybrid Dual IGBT Drivers. They are rated for blocking voltages up to 1200 V, which nicely matches the chosen IGBTs. One of the most important features of the drivers is the galvanic isolation they provide between the control circuitry and the high voltage power section. Additionally, they provide short-circuit protection by V_{ce} monitoring and are rated at a switching frequency of up to 50 kHz.

3. Hall Effect Devices

The Hall effect devices are LEM LA 200-P current transducers. This board mounted transducer has a primary current range of $0-300$ A, accurately follows 200 A/μs, and has a frequency bandwidth of dc -100 kHz (-1 dB). Figure 10 shows the Hall effect devices mounted along side the IGBTs. The Hall effects produce a current that is converted to a voltage via a burdening or measuring resistor. The manufacturer specifies an acceptable range of measuring resistors from $0-60$ Ω. However, the inverter was first tested at low current, requiring resistor values outside the acceptable range. A resistor value of 2 kΩ will result in a 1 V output when measuring 1 A of current (i.e., 1 kΩ yields 0.5 V for 1 A). Thus, by selecting the appropriate measuring resistor, the output could be scaled, allowing the use of low voltage circuitry to control a large load current.

4. Delay Times

Each component (including those in the control circuitry) has a response and/or propagation delay time which is listed on its data sheet. Those values are summarized in Table 3. The circuit, driver, and IGBT delays have an effect on the inverter output. Once the load current reaches a hysteresis boundary, it will take some time for that event to trigger the appropriate switching. The delay will allow the load current to actually travel outside the hysteresis band before the IGBTs are switched and the current is forced back into the band. The result is a slightly wider hysteresis band and, therefore, a slightly lower switching frequency. Summing those values in Table 3 gives an estimated delay of less than $3\ \mu s$ per switching. Taking the reciprocal yields a maximum switching frequency of 333 kHz for the controller. Beyond this value the circuit delays will dominate and not allow further control of the load current. As noted above, there are no COTS drivers that could approach 333 kHz, so this is not an issue for this application. However, limiting f_{max} to 10 percent, or 33 kHz, ensures the control circuitry and drivers do not unduly limit controllability.

Component	**Delay Time**	**Units**
LM319 Dual High-Speed Comparator	80	ns
CD4001 Nor Gates (Used for Flip-Flop)	280	ns
Drivers	1	µs
IGBTs	650	ns
Hall Effects	< 1	µs

Table 3. Component Delay Times.

B. COMPUTER SIMULATION

Although all components are capable of operating at 50 kHz, a cap of 33 kHz is established due to circuit delays. The actual switching frequency is primarily dependent on the hysteresis band, dc bus voltage, and load impedance. To assist in selecting the

proper values for these parameters, a MatLab program was written to determine the maximum switching frequency and power losses based on load impedance, hysteresis band, and dc bus voltage. The inductor used for the load is a 42.5-mH inductor with several taps ranging from 5% to 100% in 5% increments, which served as a basis for choice of inductor values. Additionally, the simulation incorporates the estimated circuit delay of 3 μs per switching. Power losses are calculated in the program and are presented in the section on full power simulation.

1. Modeling the Controller

Although the inverter is a three-phase device, the simulation was performed for a single-phase. The controller handles each phase independently, so simulation of a single-phase is sufficient to show the basic operation of the inverter. In order to model the controller in MatLab, equations for the load current must be established. The equations are based on a single-phase of the half-bridge configuration shown in Figure 8. Two possible switching schemes exist, a two-state and a three-state. The first option is to switch both transistors at the same time, so one is always "on" while the other is "off". This ensures either V^+ or V^- is always applied to the load. The experimental phase of this thesis used a controller designed for this type of switching.

A second and arguably better option is to allow a third state or "zero" voltage state [5]. This state is accomplished by turning both transistors "off" and allowing the load current to continue through the substrate diode. To help visualize this concept, consider the positive slope of the sinusoidal load current and refer to the half-bridge circuit in Figure 8. The upper switch, S_1, turns "on" when the load current reaches the lower boundary of the hysteresis band and drives the current higher towards the upper boundary of the band. When the load current reaches the upper boundary, S_1 turns "off". Rather than turn "on" the lower switch, S_2, and drive the current back down to the lower boundary, it is left "off" and the current is allowed to decay through the substrate diode of S_2. When the load current again reaches the lower boundary of the hysteresis band, S_1 again turns "on". For the negative slope of the output, the switching roles are reversed to drive the current in the negative direction. The benefit of this option is lower switching frequency, thus lower switching losses. However, implementing this type of switching is a

bit more complicated because it requires the use of a cross-over detector to determine the active switch in each half-bridge. The controller designed for the experimental phase of this thesis is a two-state. However, the three-state was modeled in the MatLab simulation to compare it to the method actually implemented.

Consider the case when switch S_1 is closed and S_2 is open. The voltage across the load is

$$V^+ = v_L + v_R, \tag{4.8}$$

where v_L is the voltage across the inductor, and v_R is the voltage across the resistor. The inductor and resistor voltages can be written as

$$v_L = L\frac{di_L}{dt} \tag{4.9}$$

and

$$v_R = i_L R, \tag{4.10}$$

where L is the load inductor value, i_L is the current through the inductor, and R is the resistor value. Substituting Equations (4.9) and (4.10) into (4.8) and rearranging yields

$$\frac{di_L}{dt} = -\frac{R}{L}i_L + \frac{V^+}{L}. \tag{4.11}$$

(If switch S_1 is open and S_2 is closed, the equation will be similar, but with V^+ replaced by V^-.) Equation (4.11) is a differential equation with the solution

$$i_L(t) = e^{\frac{-R}{L}(t-t_0)} i_L(t_0) + \int_{t_0}^{t} e^{\frac{-R}{L}(t-\tau)} \frac{V^+}{L} d\tau. \tag{4.12}$$

Equation (4.12) can be reduced to

$$i_L(t) = e^{\frac{-R}{L}(t-t_0)} i_L(t_0) + \frac{V^+}{R}\left(1 - e^{\frac{-R}{L}(t-t_0)}\right). \tag{4.13}$$

Again, the equation for the case where switch S_1 is open and S_2 is closed is similar, but with V^+ replaced by V^-,

$$i_L(t) = e^{\frac{-R}{L}(t-t_0)} i_L(t_0) + \frac{V^-}{R}\left(1 - e^{\frac{-R}{L}(t-t_0)}\right). \tag{4.14}$$

For the zero voltage state the load current is

$$i_L(t) = e^{\frac{-R}{L}(t-t_0)} i_L(t_0). \tag{4.15}$$

Equations (4.13), (4.14), and (4.15) are needed to model the controller in MatLab. The MatLab script files are shown in Appendices A and B.

2. Computer Simulation Results

Based on the modeling Equations (4.13), (4.14), and (4.15), MatLab script files were written to simulate the controller under both two-state and three-state switching. Figure 11 is a MatLab plot showing the load current contained within a 0.4 A hysteresis band ($I_h = 0.2$ A) using the two-state switching. Figure 12 is a similar plot, but with the zero voltage state allowed. Parameters for the simulation were as follows: $L = 0.0105$ H, $i_{\text{ref}} = 2\sin(377t)$ A, $I_h = 0.2$ A, $V^+ = 10$ V, and $V^- = -10$ V. The figures reveal that the switching frequency is greater in the peak and valley of the waveform. The maximum switching frequency with the two-state is 1.2 kHz, compared to 730 Hz for the three-state.

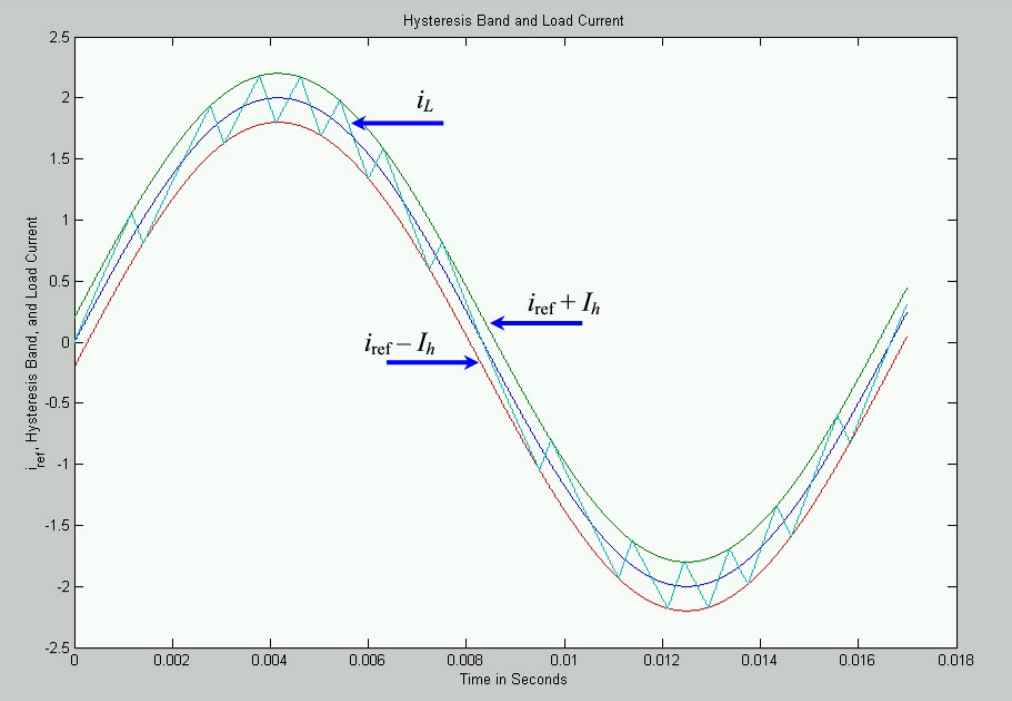

Figure 11. MatLab Simulation of Load Current ($I_h = 0.2$ A).

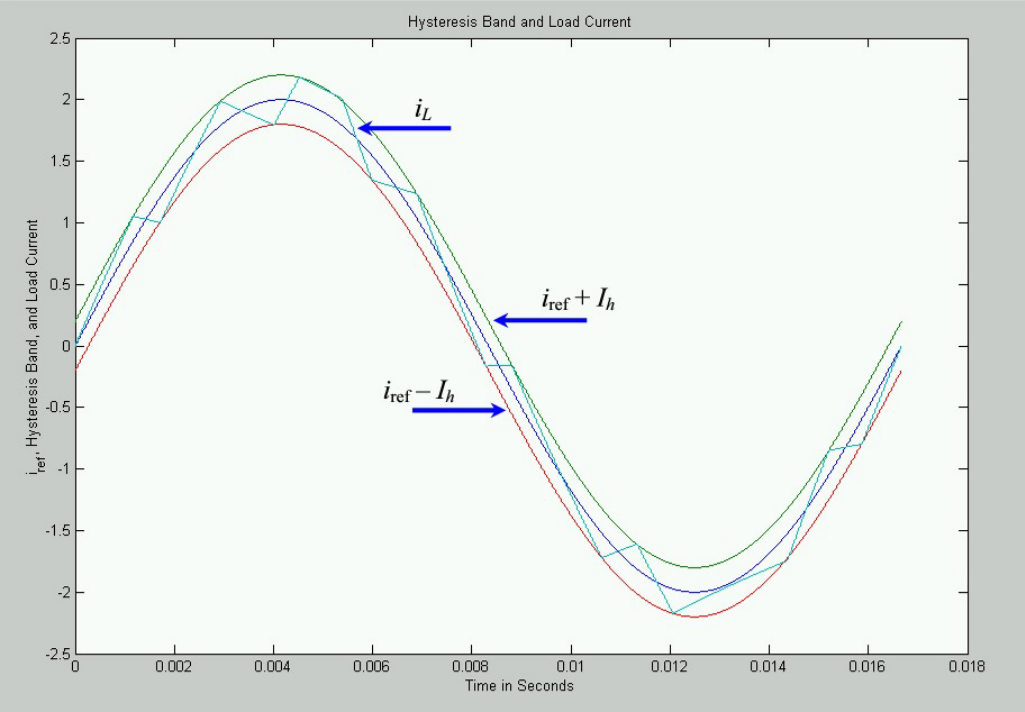

Figure 12. MatLab Simulation of Load Current Using Three-State Switching ($I_h = 0.2$ A).

If the hysteresis band is narrowed to 0.08 A ($I_h = 0.04$ A), but all other parameters remain unchanged, $f_{\max}$ becomes 5.6 kHz for the two-state and 3.1 kHz for the three-state. Figures 13 and 14 show the MatLab plots using the narrower band. There is a noticeable improvement over the wider band plots of Figures 11 and 12.

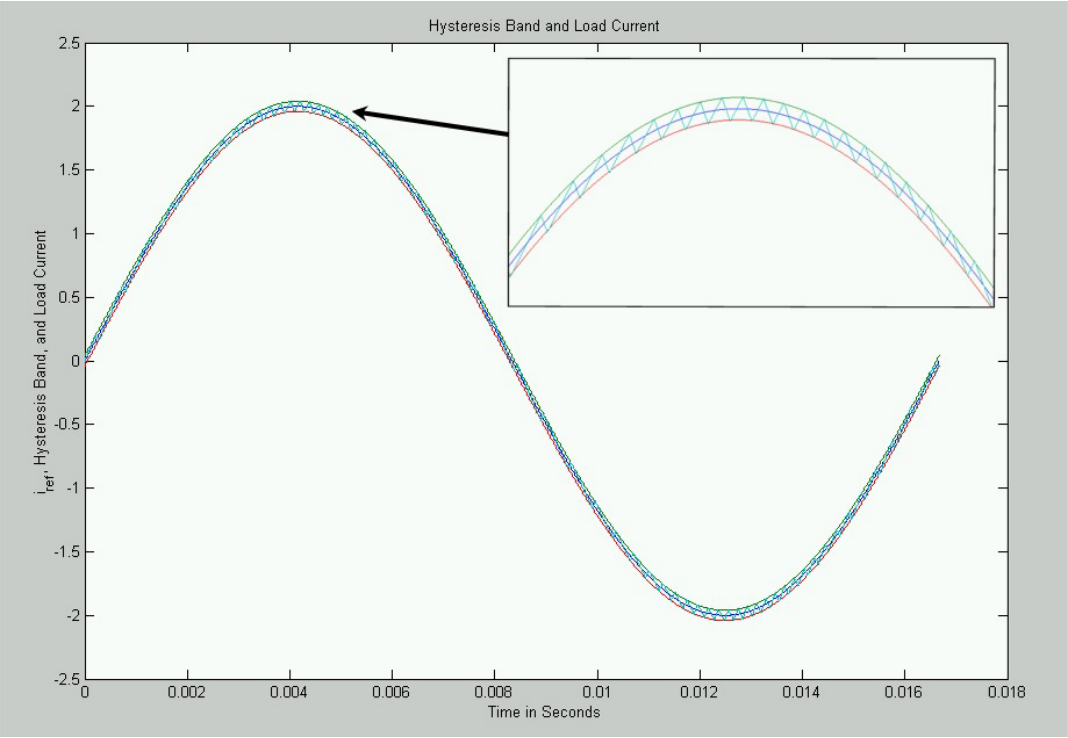

Figure 13. MatLab Simulation of Load Current ($I_h = 0.04$ A).

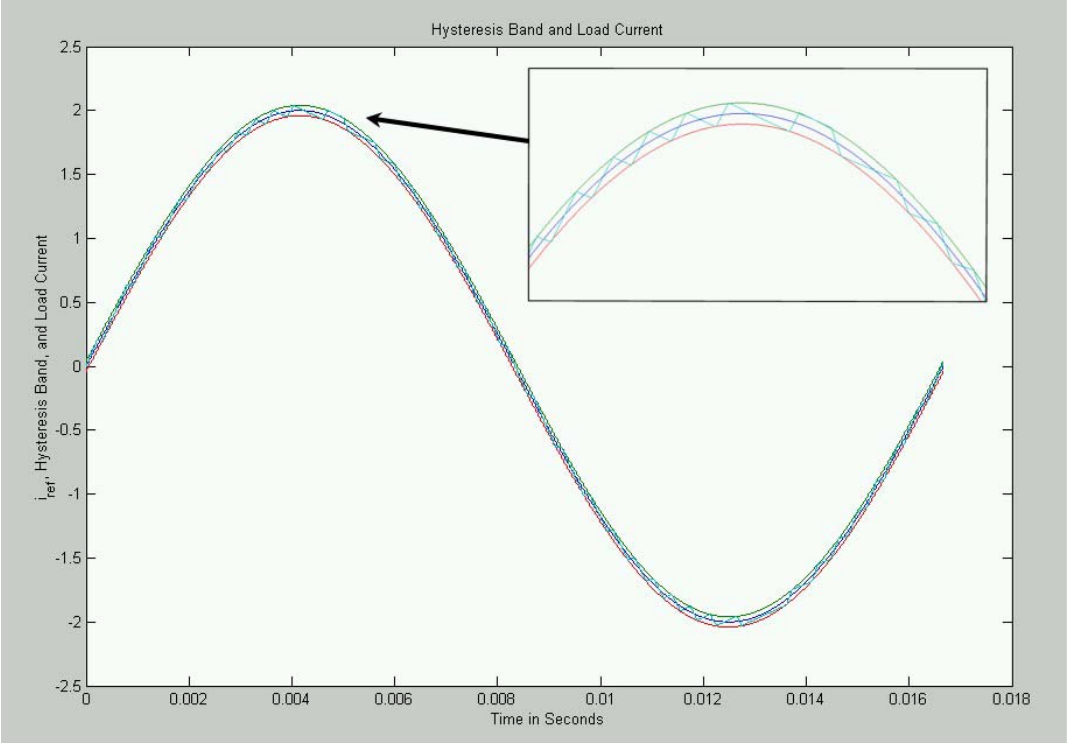

Figure 14. MatLab Simulation of Load Current Using Three-State Switching ($I_h = 0.04$ A).

Table 4 shows several values for inductance, hysteresis band, and associated maximum switching frequencies. The values in Table 4 are used for the experimental testing of the inverter. Since the actual controller was designed to utilize two-state switching, the zero voltage state results are omitted from Table 4. However, previous results indicate that $f_{\max}$ would be about half. The calculations were based on a 2-A_{peak}, 60-Hz reference sine wave, and a load resistance of $R = 1\ \Omega$. The average switching frequency is labeled f_{avg}.

f_{max} (kHz)	f_{avg} (kHz)	I_h (A)	L (mH)	V^+ (V)	V^- (V)
1.41	1.02	0.2	9.1	10	−10
2.71	1.98	0.1	9.1	10	−10
4.40	3.24	0.06	9.1	10	−10
11.83	8.76	0.02	9.1	10	−10
18.15	12.30	0.02	7	10	−10
32.17	20.94	0.01	7	10	−10

Table 4. Switching Frequencies for Various Hysteresis Bands and Load Inductance.

C. FULL POWER SIMULATION

The inverter is designed for the ratings shown in Table 5.

Rating	Value
Maximum Real Power	50 kW (water-cooled), 30 kW (air-cooled)
Maximum dc Link Voltage	750 V
Maximum Output RMS Voltage	450 V (line-to-line) @ 0–60 Hz
Maximum Output RMS Current	80 A (0.8 power factor)
Power Factor	0.8 Lagging (worst case)

Table 5. Inverter Ratings.

In order to operate the inverter at full power, the measuring resistor for the Hall effect device should be within manufacturer's specifications and limit the feedback signal, i_{out}, applied to the control circuitry. At rated power, the load current is 92 A_{peak}. The Hall effect devices have an output/input ratio of 1/2000 A/A, so the output from the Hall effect device is $92 \times 1/2000 = 0.046$ A_{peak}. A 60 Ω measuring resistor will ensure that i_{out} (feedback signal) remains below 3 V, where the conversion factor would be 30 mV/A.

1. Simulation Results

The values from Table 5 were used to simulate one phase of the inverter at full power. Table 6 shows the results of the MatLab simulation for several values of I_h, R, L, and associated Displacement Power Factor (DPF). The total power losses, P_{tot}, are also shown in the table. Recall that the IGBTs can dissipate 1500 watts, which is well above anything achieved during simulation.

$f_{\max}$ (kHz)	f_{avg} (kHz)	P_{tot} (Watts)	I_h (A)	R (Ω)	L (mH)	DPF
7.34	3.36	285	2	3.3	6.375	0.81
14.18	6.24	394	1	3.3	6.375	0.81
23.58	10.38	414	1	3.3	4.25	0.90
29.70	14.16	505	0.75	3	4.25	0.88

Table 6. Switching Frequencies for Full Power Simulation.

Figure 15 shows the MatLab plot for the latter case, $I_h = 0.75$ A, $R = 3\ \Omega$, and $L = 4.25$ mH. The window in Figure 15 shows the undershoot caused by the 3-μs circuit delay. Notice that at the positive peak the current travels farther below the band than above the band. This is due to a combination of circuit delays and voltage across the inductor. When the negative rail voltage is applied at the peak, most of the voltage drop is across the inductor causing an extreme d_i / d_t and more undershoot below the lower boundary. The opposite is true at the negative peak and the load current travels further outside the upper boundary. The greater the $|d_i / d_t|$ at the band limits, the greater the over or undershoot. The amount of distortion in the current waveform is quantified by means of the Total Harmonic Distortion (THD) and is computed in the MatLab program.

The THD (in percent) is computed by

$$\%\text{THD}=100\times\sqrt{\frac{\sum_{k=2}^{\infty} I_k^2}{I_1^2}}, \tag{4.16}$$

where I_k is the rms value of the Fourier series component at the k^{th} harmonic frequency and I_1 is the rms value of the fundamental component [8]. The current waveform in Figure 15 has $\text{THD}=1.23\%$.

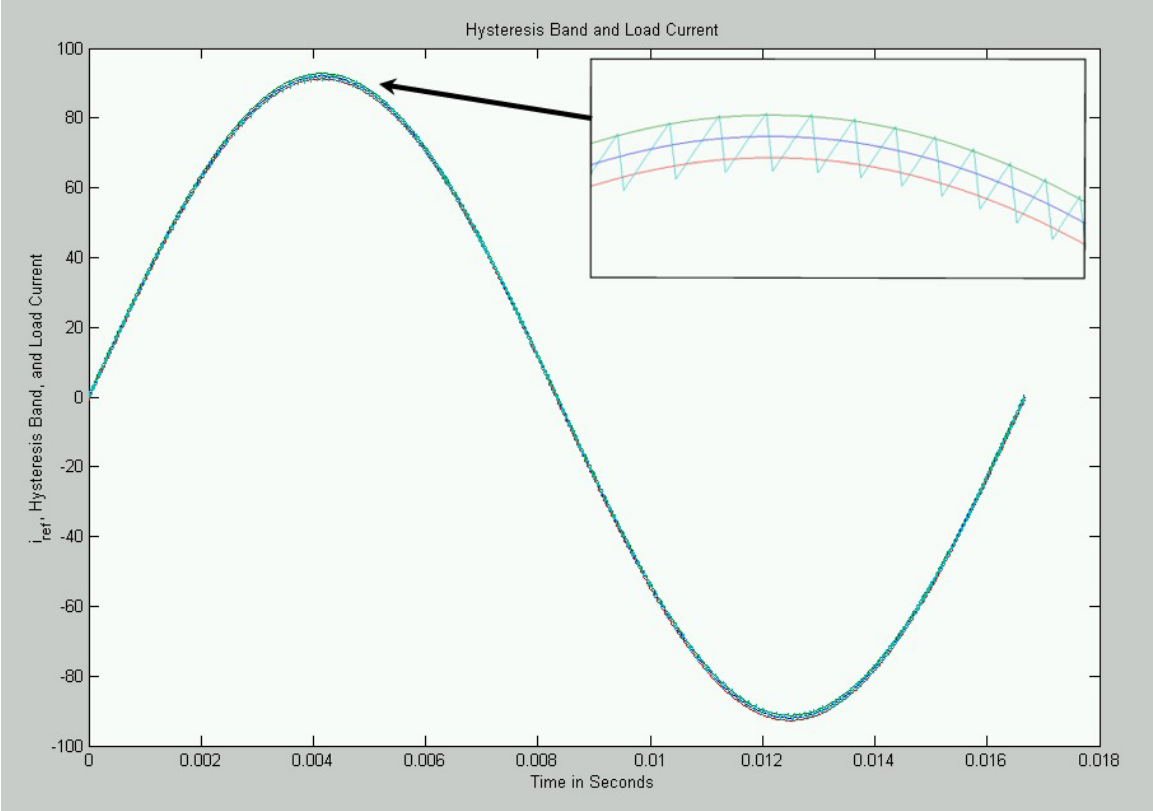

Figure 15. Full Power Simulation.

By implementing the zero voltage state, a better DPF was achieved at lower switching frequencies, as shown in Table 7. Utilizing the three-state model results in significantly lower switching frequencies and power losses due to extensive use of the substrate diode. Notice that the power losses were reduced slightly when I_h was reduced

from 1 A to 0.75 A. Generally, switching losses account for most of the power losses in a half-bridge circuit. However, conduction and diode losses dominate at the wider band and the switching losses are only a small portion due to the low switching frequency and use of the substrate diode. At narrower bands, switching losses begin to dominate, but the conduction and diode losses are reduced. Near $I_h = 0.75$ A a balance in losses is reached for this *RL* load. Figure 16 is the associated plot for $I_h = 0.75$ A, $R = 2.7\ \Omega$, and $L = 2.125$ mH. The window in the plot shows evidence of the circuit delays allowing the load current to travel outside the hysteresis band.

f_{max} (kHz)	f_{avg} (kHz)	P_{tot} (Watts)	I_h (A)	R (Ω)	L (mH)	DPF
9.55	2.88	16.5	1	2.7	4.25	0.86
12.26	3.72	15.6	0.75	2.7	4.25	0.86
17.37	6.9	22.4	0.75	2.7	2.125	0.96

Table 7. Switching Frequencies, Full Power With Three-State Switching.

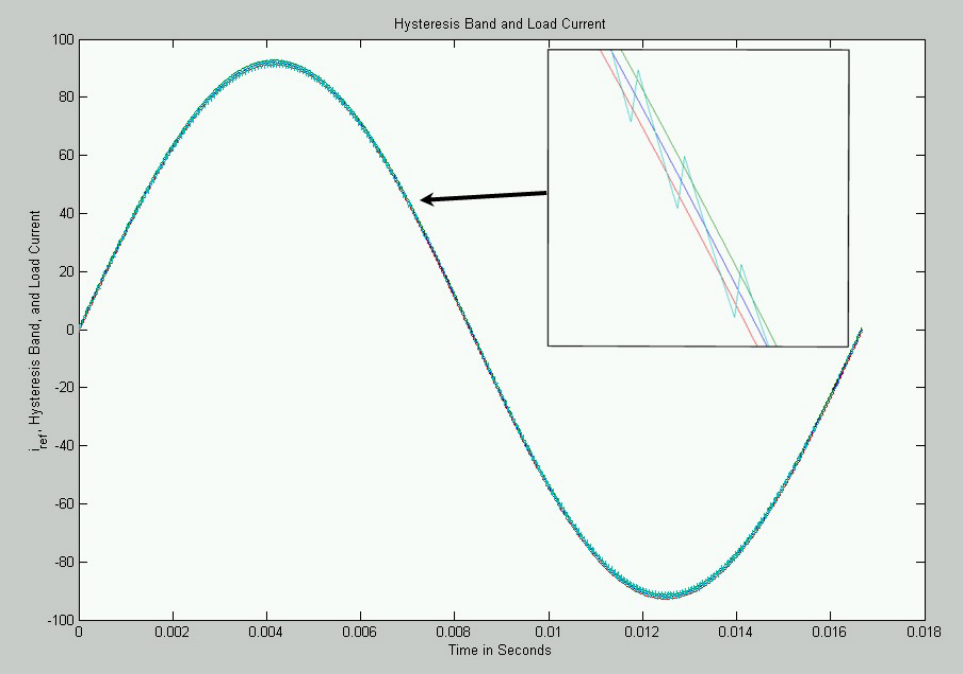

Figure 16. Full Power, Three-State Switching.

D. SUMMARY

Computer simulation shows that hysteresis control has merit. Two switching schemes have been presented, the first method ensures one of the switches is always "on" and the second uses a zero voltage state. Implementing two-state switching on the controller is less complicated, but a wider hysteresis band must be used to limit the switching frequency. On the other hand, utilizing three-state switching significantly reduces the switching frequency and power losses, but designing and building such a controller is a bit more complicated due to the necessity of a crossover detector. The next chapter presents the results of the physical experiment.

V. EXPERIMENTAL RESULTS

This chapter discusses the testing of the inverter. Single-phase, three-phase, and parallel test results and oscilloscope displays are presented. Simulation values from Table 4 are used to draw a comparison to experimental results.

A. PRELIMINARY TESTING

Prior to testing the inverter, several aspects (i.e., bus voltages, reference signal, hysteresis band, IGBT drivers, etc.) were measured or tested to ensure the circuit components were functioning according to the manufacturer's specifications. In the process of evaluating the individual components, various anomalies and characteristics were noted and are discussed in the text below.

1. IGBT Drivers

The drivers provide galvanic isolation between the control circuitry and the power section. Testing revealed severe degradation of the switching signals on the control side when current was applied to the power section. The problem was isolated to the V_{ce} monitoring, which was false triggering due to circuit timing issues. The V_{ce} monitoring is a feature on the drivers that shuts-down the gating signal in the event that a short-circuit is detected on the power side. However, it was not designed to operate effectively with all control and converter topology combinations. Since the hysteresis control has an inherent short circuit protection, this feature on the drivers was deemed unnecessary and it was disabled. After disabling the V_{ce} monitoring, the drivers worked flawlessly.

2. Inductors

All the inductors were rated at 42.5 mH with coil taps at 5% intervals. Three matched inductors were found that measured 9.1 mH on the 30% tap and were used for the experiment. It should be noted that the inductors are constructed with laminated iron cores and have no air gap. Thus, inductance varies widely over frequency.

3. Hall Effect Devices

An interesting problem regarding magnetization of the Hall effect devices was encountered and should be duly noted for low power testing. Upon power-up and prior to

applying any voltage or current to the load, the output from the Hall effects should have been zero. However, the output was about 0.5 mA, which is twice the 0.25 mA maximum listed in the specification sheet. The 0.5 mA output resulted in a 1 V drop across the 2 kΩ measuring resistor. At full power (a load current of 65 A_{rms} or 92 A_{peak}) a 0.5 mA offset is much less significant due to a smaller measuring resistor (<60 Ω). With the low current (<3 A) and large measuring resistor (2 kΩ) used for initial testing, the offset is unacceptable. This offset was due to magnetization of the Hall effects, possibly caused by a current spike from a previous experiment. To solve this problem, a capacitor was charged and rapidly discharged creating a large current flow through the Hall effects to reverse the magnetization and bring the offset within manufacturer's specifications. After the offset was brought within manufacturers specifications (<0.25 mA), it was still deemed unacceptably large for low current testing. The primary factor is the large measuring or burdening resistor required for low current testing (0.2 mA across a 2-kΩ resistor is 0.4 V). To mitigate the effects of the offset, the current through the Hall effect sensors was virtually multiplied by looping the wire several times. Each loop through the Hall effect device adds to the sensed current. For example, two loops doubles the sensed current, three loops triples the sensed current, and so on. The wire was looped through the Hall effects 20 times, so a 2-A_{peak} sine wave appeared to be a 40-A_{peak} sine wave. Because the current was multiplied 20 times, the measuring resistor was reduced by the same factor, or divided by 20. So the 2-kΩ measuring resistor was replaced with a 100-Ω resistor, which is much closer to the manufacturer's recommendation of $0-60$ Ω. Thus the offset seen by the control circuitry was reduced to 0.02 V. Looping the wire through the Hall effect device adds 16 μH of series inductance to the load (an insignificant value compared to $L = 9.1$ mH).

B. SINGLE PHASE TESTING

Testing was performed based on the values in Table 4, where $i_{ref} = 2\sin(377t)$ A and $R = 1$ Ω. The results are shown below in Table 8 without the average switching frequency, f_{avg}. The average switching frequency is important to consider if f_{max} exceeds the nominal switching frequency of the IGBTs (because f_{avg} may then exceed the nomi-

nal switching frequency of the IGBTs) or in calculating power losses. Neither of these is a factor for this level of testing, so f_{avg} was not determined.

f_{max} (kHz)	I_h (A)	L (mH)	V^+ (Volts)	V^- (Volts)
1.25	0.2	9.1	10	–10
2.38	0.1	9.1	10	–10
4.31	0.06	9.1	10	–10
15.63	0.02	9.1	10	–10

Table 8. Single-Phase Test Results.

Figures 17–20 show the oscilloscope display for each of the rows in Table 8. Notice the vertical scale set to 20 mV in each of the figures. The readings were taken via a 1/50 V/V differential probe. Since the 1-Ω load resistor is used to monitor the output current, each division on the scope equals 1 A.

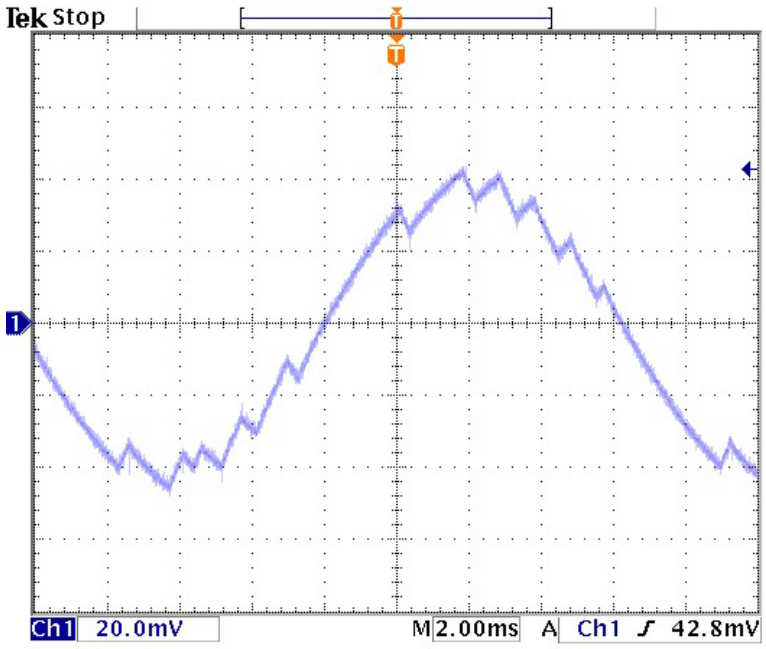

Figure 17. Single-Phase Scope Display (1 A/div, $I_h = 0.2$ A).

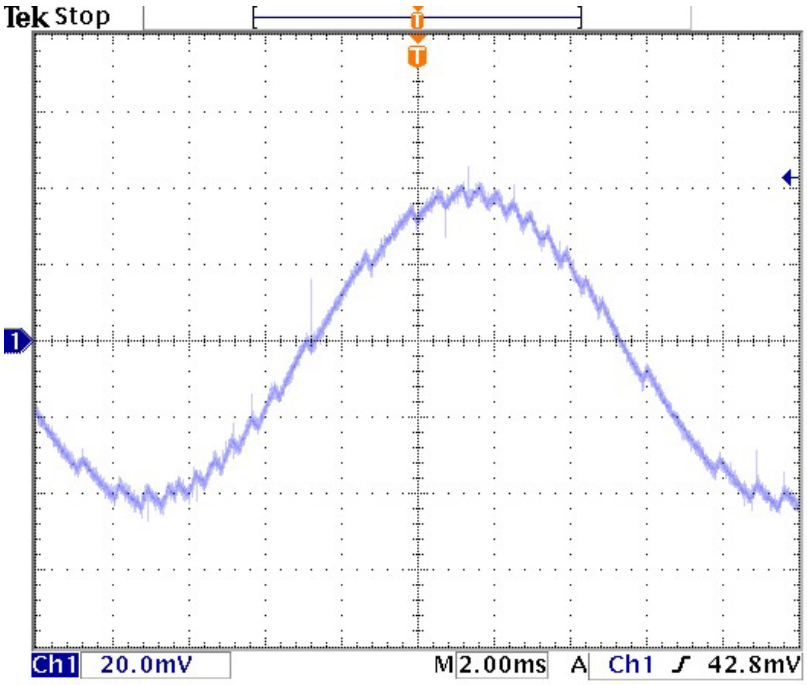

Figure 18. Single-Phase Scope Display (1 A/div, $I_h = 0.1$ A).

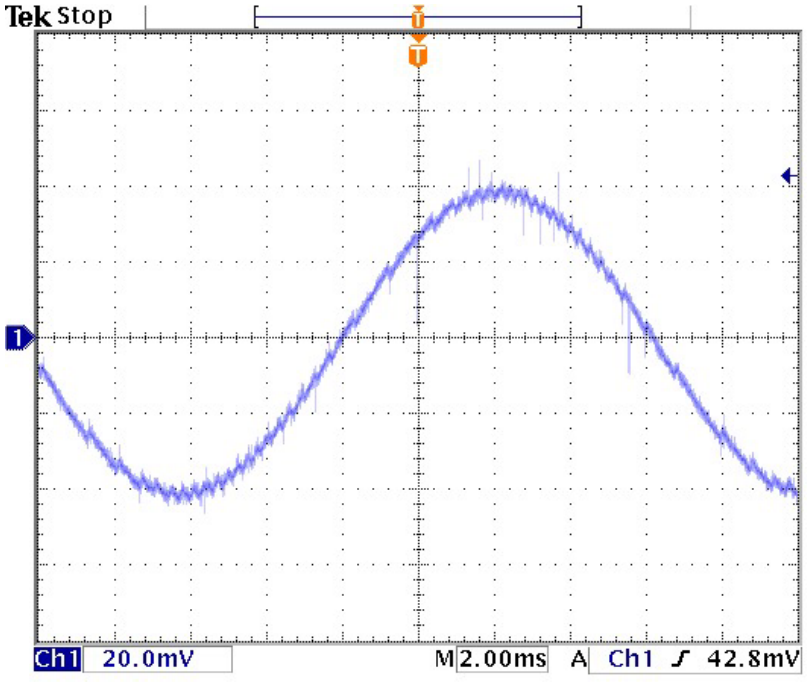

Figure 19. Single-Phase Scope Display (1 A/div, $I_h = 0.06$ A).

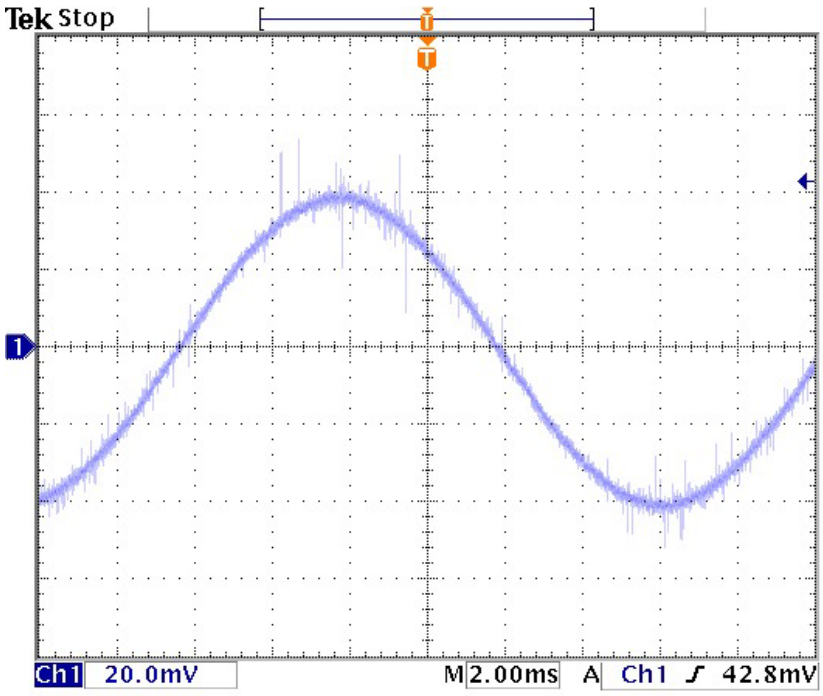

Figure 20. Single-Phase Scope Display (1 A/div, $I_h = 0.02$ A).

Comparison between Tables 4 and 8 shows the experimental results closely match those of the simulation. However, there is some discrepancy in the maximum switching frequency, $f_{\max}$. At the wider hysteresis bands, $f_{\max}$ is actually lower in the experiment than in the simulation. As the hysteresis band is narrowed, $f_{\max}$ becomes higher than in the simulation due to the decrease in inductance at higher frequencies. The laminated, non-air gap iron core inductor is frequency dependent, where L decreases as f_s increases. The decrease in L causes an increase in $f_{\max}$ beyond what was predicted in the simulation. An attempt was made to reduce the hysteresis band below 0.02 A, but the switching frequency became so high that the drivers shut down. Thus, $I_h = 0.02$ A is the practical minimum under the load parameters in Table 8.

C. THREE-PHASE TESTING

In order to test three-phase operation, a three-phase reference signal is necessary. The three-phase reference was generated digitally. Three Programmable Logic Devices (PLD) were used to output a 36-step sine wave, each one separated by 120 degrees. The

output of each PLD was fed through a resistor tree, filtered, and amplified to produce the three-phase reference signal. A wiring diagram of the three-phase generator circuit is displayed in Appendix C.

The power section of the circuit was assembled as in Figure 8. Figures 21–24 show all three phases of the output current on one oscilloscope. The parameters for each phase are the same as those used for the single-phase case in Figures 17–20 ($R = 1\ \Omega$, $L = 9.1$ mH, $V^+ = 10$ V, and $V^- = -10$ V).

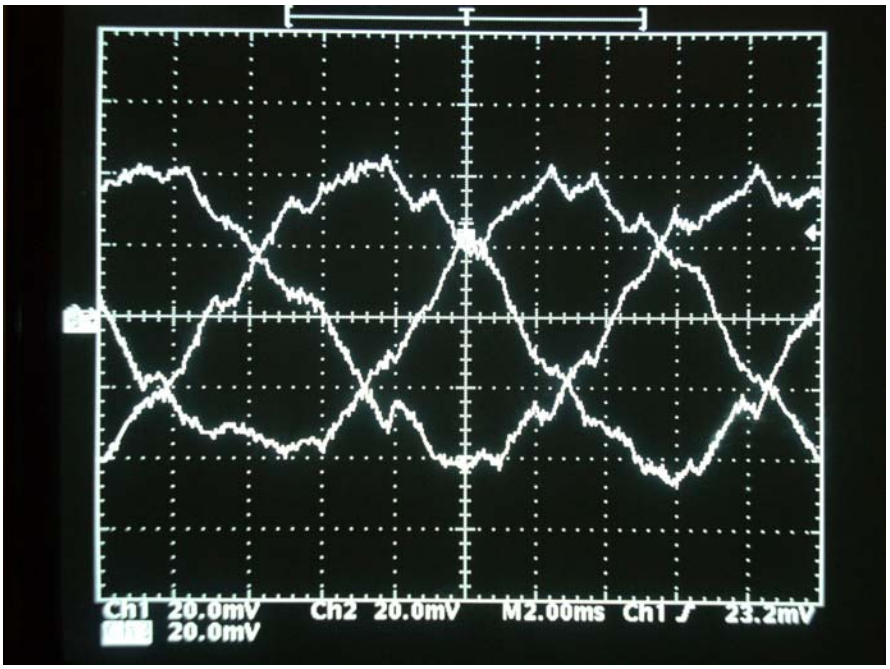

Figure 21. Three-Phase Scope Display (1 A/div, $I_h = 0.2$ A).

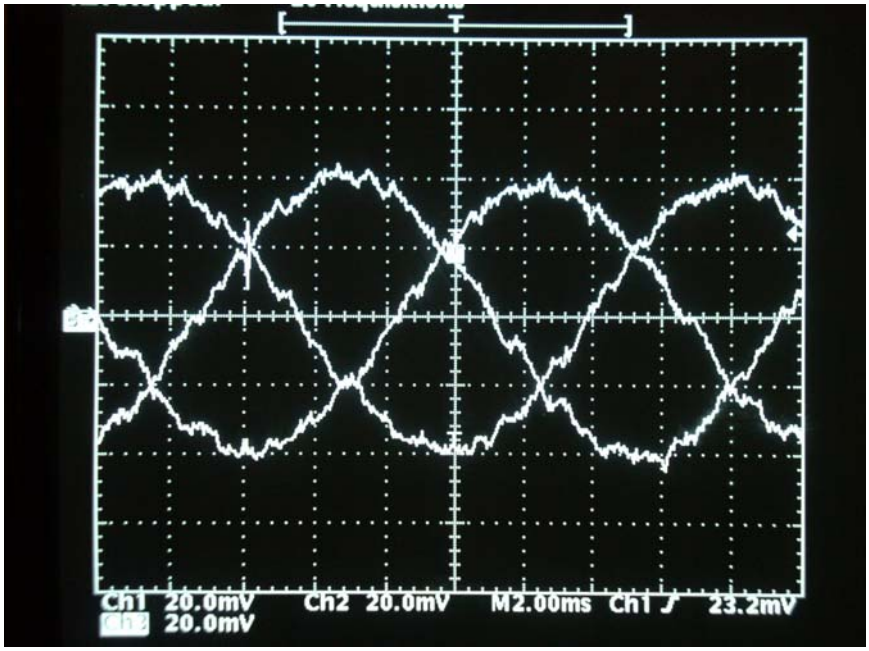

Figure 22. Three-Phase Scope Display (1 A/div, $I_h = 0.1$ A).

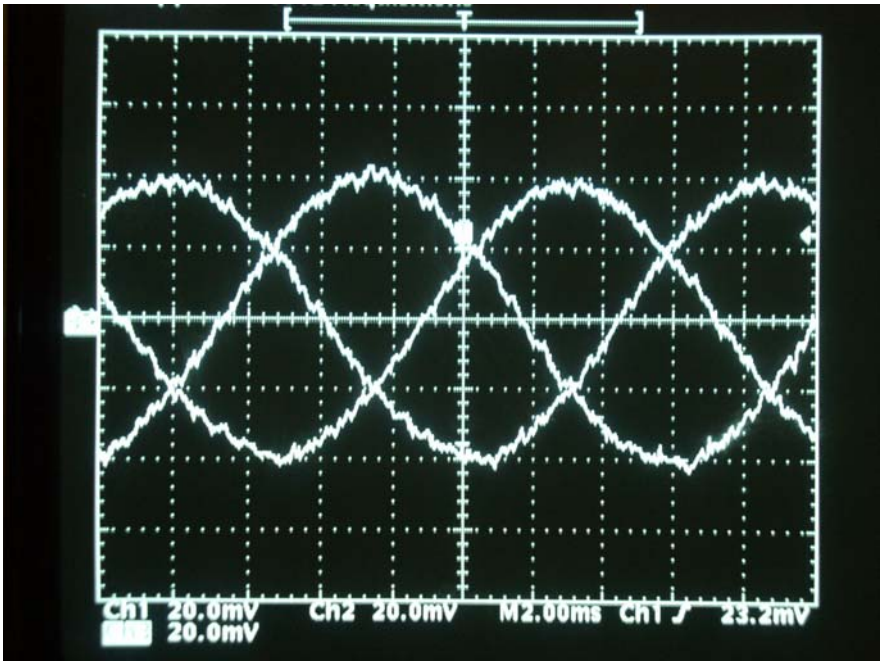

Figure 23. Thee-Phase Scope Display (1 A/div, $I_h = 0.06$ A).

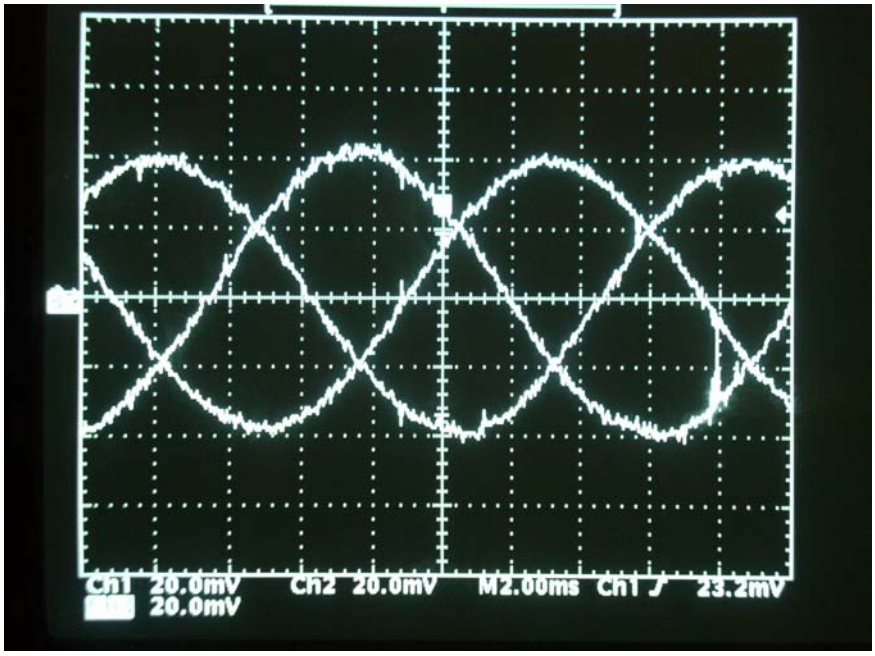

Figure 24. Three-Phase Scope Display (1 A/div, $I_h = 0.02$ A).

D. PARALLEL TESTING

Figure 25 is the simplified block diagram of two inverters in parallel. In theory, the bulk inverter provides most of the current to the load and the high fidelity inverter shapes the load current into a sinusoidal waveform. This method of load sharing requires different sized combining inductors at the output of each inverter based on inverter size and output load impedance.

A single-phase parallel test was performed in which the bulk inverter consisted of a signal generator feeding an LM12CL (an 80-W operational amplifier capable of producing ± 25 V and ± 10 A) [14]. The magnitude of the output voltage was controlled by the amplitude of the square-wave input to the LM12CL. A single phase of the hysteresis controlled inverter built for this thesis was used to mimic the high fidelity inverter. This inverter is easily capable of producing low-distortion sine waves. For the test performed in this thesis, both inverters were of equal power. Figure 26 is the simplified diagram of the actual paralleling test configuration.

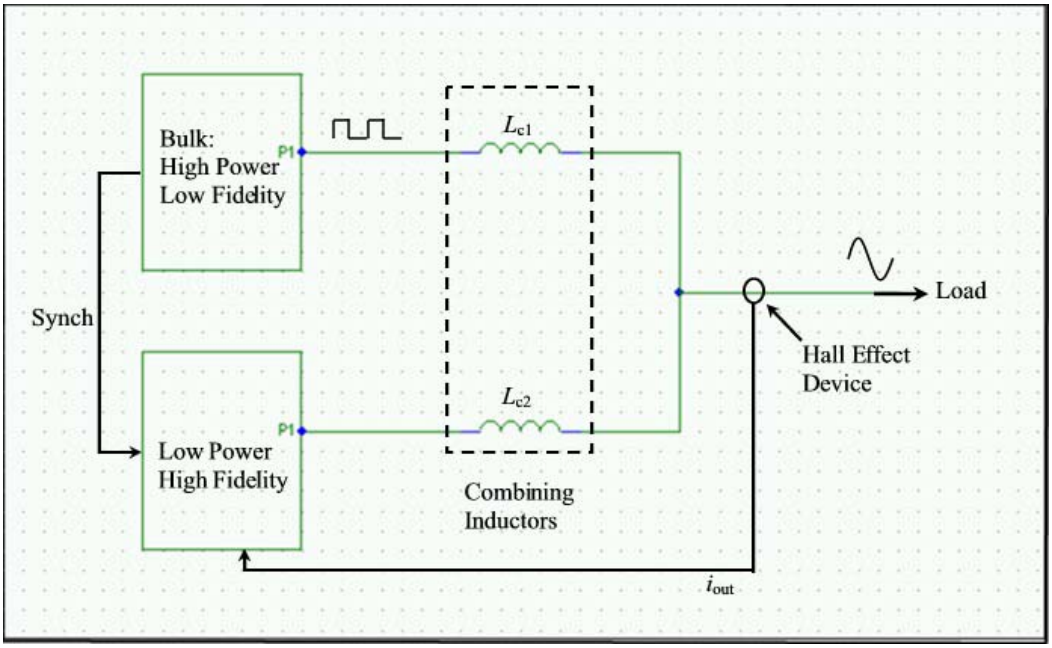

Figure 25. Simplified Block Diagram of Paralleled Inverters.

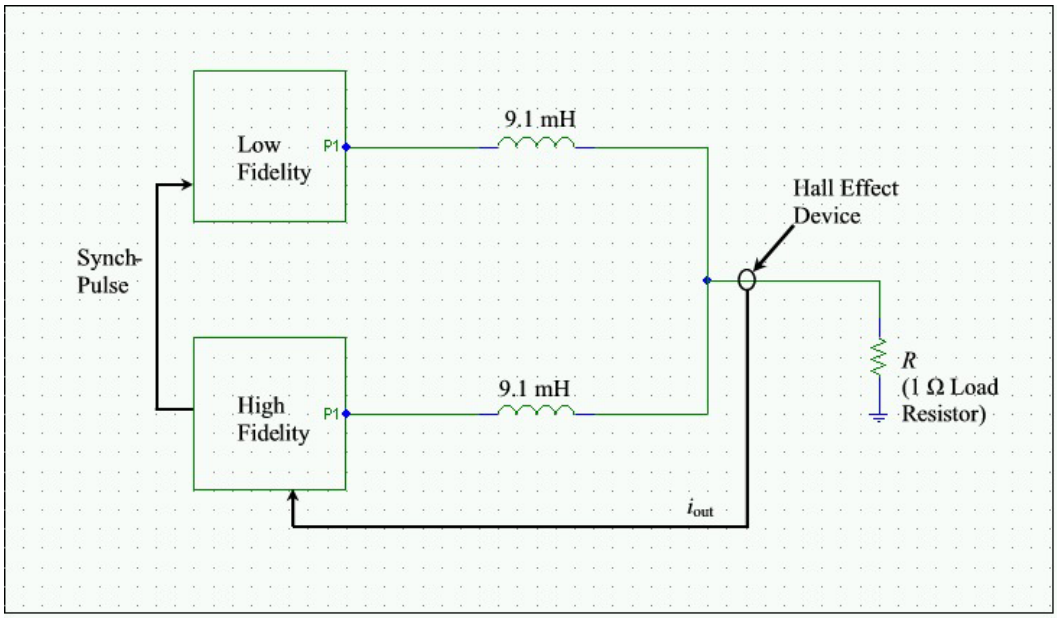

Figure 26. Simplified Block Diagram of Parallel Test Configuration.

For parallel testing, the hysteresis controller was programmed with $I_h = 0.1$ A and $i_{\text{ref}} = 2\sin(377t)$ A. Figure 27 shows the load current and the high fidelity (hysteresis controlled) inverter current. Figure 28 displays the load current and the low fidelity

inverter current. These two figures demonstrate the load sharing capability of the parallel architecture where the output current is the summation of the low and high fidelity currents. The bulk inverter provides the majority of current to the load and the high fidelity inverter provides the small amount necessary to shape the output into a sinusoidal waveform. Figure 29 displays the load current and bulk inverter voltage. The two waveforms are about 90° out of phase. This phase shift is purposefully set to take advantage of the current lag introduced by the bulk inverter inductor and optimally synchronize the output current of the two inverters.

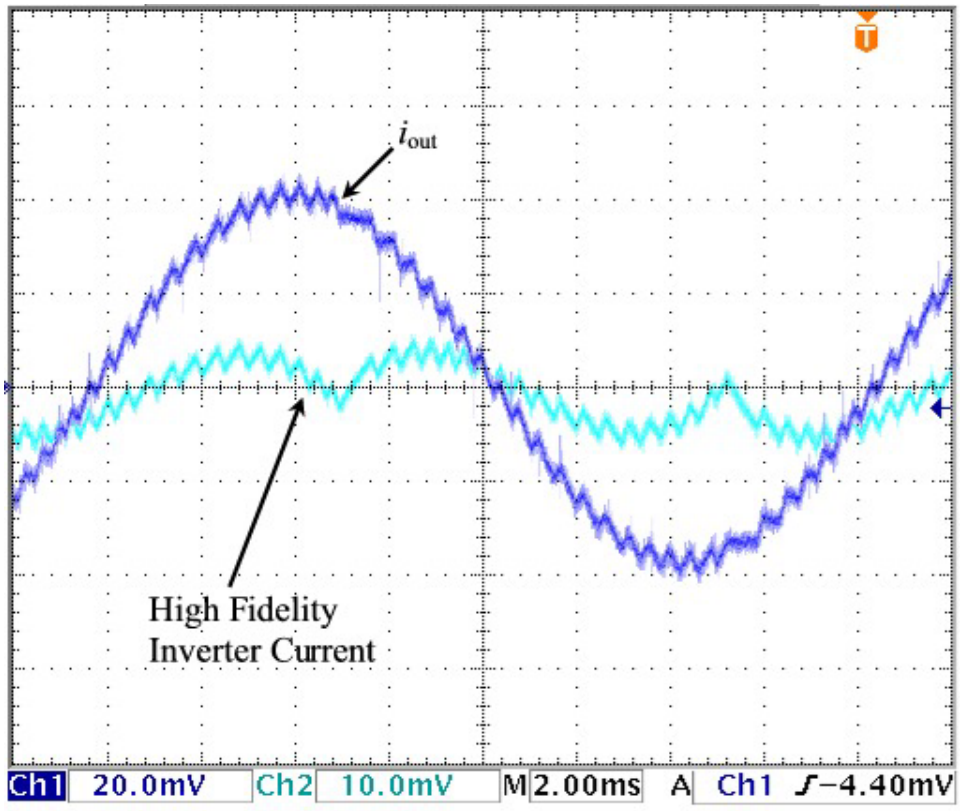

Figure 27. Load Current and High Fidelity Inverter Current (1 A/div).

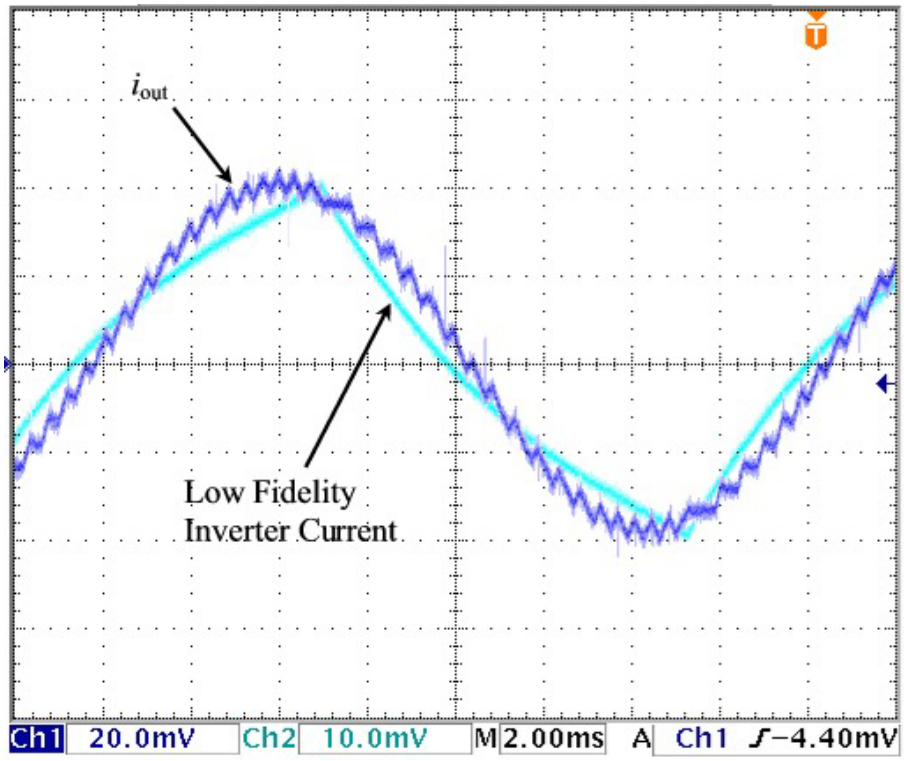

Figure 28. Load Current and Low Fidelity Inverter Current (1 A/div).

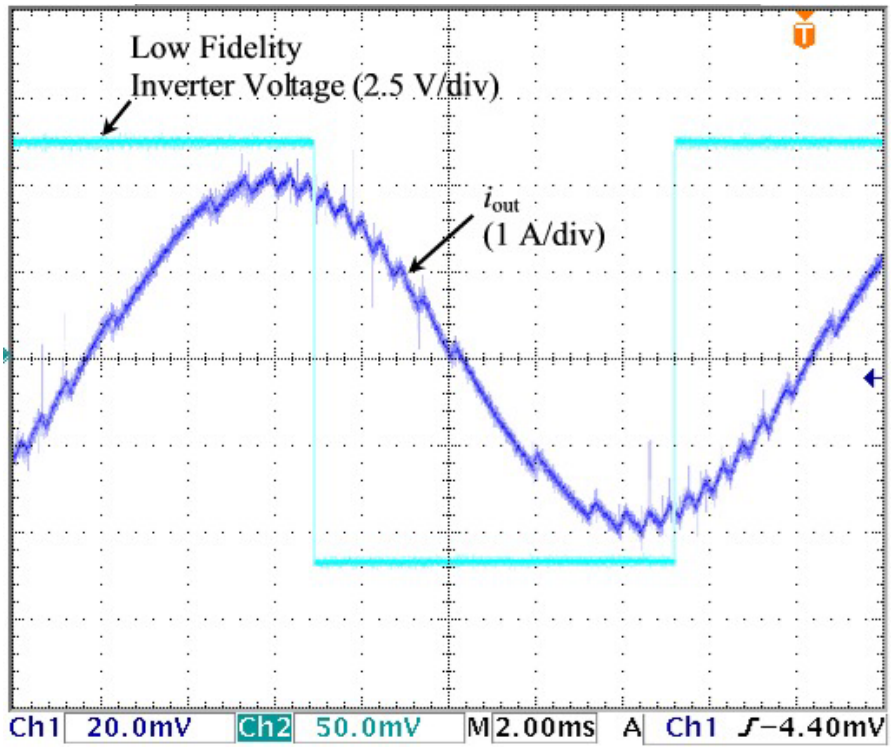

Figure 29. Load Current and Bulk Inverter Voltage.

E. SUMMARY

As a stand-alone unit, the hysteresis controlled inverter produces a sinusoidal load current. The simulation for predicting switching frequency based on load impedance, dc-link voltage and hysteresis band was successfully verified by the laboratory results of this chapter. The inverter was tested in both single- and three-phase configurations. After the stand-alone testing was complete, parallel testing was performed.

The parallel test demonstrated that a high fidelity low power inverter could be used to vastly improve the output waveform of a low fidelity bulk inverter. In fact, the hysteresis controlled inverter worked very well in tandem with the bulk inverter to morph the load current into a sinusoidal waveform.

The next chapter presents conclusions and recommendations for follow-on work.

VI. CONCLUSIONS

This chapter presents conclusions and recommendations for follow-on work. The main goal of this thesis was to experimentally evaluate hysteresis control in a parallel inverter topology. Test results confirm that this goal has been met.

A. SIMULATION

The simulation was a good tool for gathering data prior to testing the inverter. Two programs were written: a two-state and a three-state. The programs were written to allow the user to easily change load and inverter parameters (i.e., dc-link voltage, reference waveform structure, load impedance, circuit delays, etc.). With these two programs, almost any hysteresis controlled CSI can be simulated.

B. TESTING AT RATED POWER

Although testing was performed at low power, all circuit components for the hysteresis controlled inverter were designed and are ready for high power testing: 750-V dc-link and 65-A rms output current in a 450V line-line three-phase load. In order to conduct high power testing, sufficiently sized load elements would need to be procured. Further, 50 kW exceeds the capability of the existing switchgear and variacs in the Power Systems Laboratory. Given the acquisition of sufficiently sized load elements, a number of high-power tests can still be performed as specified in the next section.

C. FOLLOW-ON WORK

At this stage, various research avenues are apparent and there are many more interesting experiments that could be performed. Below is a list of proposed follow-on topics with a brief explanation for each. Future work should progress beginning with item 1 and continue, in order, to the last item. At the final stage, a complete evaluation of the parallel inverter topology should indicate its suitability for shipboard applications.

1. Full-Power Testing

The first step is to modify the existing bench setup to conduct testing at the 9-kW level. After this is complete, test the inverter up to the capability of the Power Systems Laboratory which is 30kW using the Stancor 450V three-phase variac. This variac is capable of testing at full voltage, but reduced current.

2. Modify the Controller from Two-State to Three-State

The controller should be modified to utilize the three-state switching method described in Chapter IV. Such a controller would enable narrower hysteresis bands, thus an improved output current waveform.

3. Construction of Additional Inverter

A second hysteresis controlled inverter should be built to perform parallel/series operation of like converters. This would help verify the modular concept for obtaining high power from combinations of low power inverters.

4. Sizing of Combining Inductors and Computing Optimal Phase Shift

Equations and methods are necessary to compute the value for the combining inductors and the phase-shift required for optimal performance. This thesis has demonstrated the possibility of paralleling two inverters for load sharing and redundancy; however, the inverters were matched in power, so equal value combining inductors were chosen. Equations and methods for sizing the combining inductors and calculating the optimal phase shift for unequal power inverters have not yet been developed.

5. Test Parallel Operation at High Power

The parallel inverter topology should be tested on an actual high power motor, such as a pump, fan, or even a 38-MW propulsion motor. This level of testing would require a high power facility and is well beyond the capabilities of the Power Systems Laboratory. The Naval Surface Warfare Center laboratory in Philadelphia would be a good location since various high power loads and power supplies are available. Additionally, integration, feasibility, and reliability studies could more easily be performed at the Philadelphia test facility to render a complete evaluation of the parallel inverter topology for shipboard applications.

D. FINAL CONCLUSION

The goals of this thesis were achieved. The hysteresis controlled inverter was designed, built, and tested with good results. Testing confirmed that hysteresis control allows for easy paralleling of inverters and that load sharing and redundancy can be achieved with this topology. Finally, a parallel architecture utilizing hysteresis controlled inverters holds promise for future use on the Navy's all electric ship.

APPENDIX A. MATLAB CODE FOR SIMULATION OF TWO-STATE INVERTER

The following code was written to simulate a single-phase hysteresis controlled inverter. The zero voltage state is not simulated in this code. The program also calculates and plots the frequency spectrum and Total Harmonic Distortion (THD) of the output current.

```
% Paul F. Fillmore
% September 2003
% Thesis - Hysteresis Band
% The object of this program is to calculate acceptable values for
% the hysteresis band, load inductance, and upper and lower rail voltage.
% A plot of the load current, reference waveform, and hysteresis band is
% generated in addition to calculating the maximum switching frequency.

%************ IMPORTANT NOTE*********************************
%  For most accurate frequency spectrum and estimation of THD, set
%  fs = 60*200000 and Tend = 12/60.
%************************************************************

h       = .2;       % half of hysteresis band
Vd      = 10;       % rail voltage should be interpreted as +Vd and - Vd.
R       = 1;        % load resistance
L       = .0091;    % load inductance
A       = 2;        % desired amplitude of load current
fs      = 60*200000;   % Sampling frequency
fn      = fs/2;      % Nyquist frequency (used for fft)
Tend    = 1/60;      % time period
t       = 0:1/fs:Tend;
iref    = A*sin(2*pi*60*t);  % reference sine wave
iupper  = iref + h;    % upper hysteresis band
ilower  = iref - h;    % lower hysteresis band

t0      = 0;
iload   = zeros(size(iref));
Delta_t = 0;
m       = 1;
k       = m;
exit    = 0;
Ic      = 0;
Id      = 0;
Delta_t_Ic = 0;
Delta_t_Id = 0;
```

```
% This next section is the meat of the program.  The load current vector is built
% using equations presented in the Thesis.  A 3microsecond delay is built into
% the switching.  Additionally, the switching period for each switching is loaded
% into a vector to later determine switching frequencies.  The variable "exit" is
% used to ensure the main "while" loop will not run indefinitely.  During the
% initial coding, an error could have resulted in the loop running indefinitely had
% the exit variable not been used.  After each switching the average current
% through the IGBT or diode is loaded into an appropriate vector.  Those vectors
% are used later to determine power losses.
while ((t0 < t(length(t))) & (exit < length(t) + 5000))
   exit            = exit +1;
   tswitch         = t(m);
   while (iload(m) < iupper(m)) & (m < length(t))
      m            = m + 1;            % Increase the index by one
      iload(m)  = exp(-R/L*(t(m)-t0))*iload(k) + Vd/R*(1 - exp(-R/L*(t(m)-t0)));
   end
   x  = m;                % Control index to establish 3microsecond delay
   while (t(m) < t(x) + 3*10^-6) & (m < length(t))
      m            = m+1;
      iload(m)  = exp(-R/L*(t(m)-t0))*iload(k) + Vd/R*(1 - exp(-R/L*(t(m)-t0)));
   end
   Icwork = (iload(k) + iload(m))/2;  % Average load current during the switching period.
   if Icwork > 0
      Ic                   = [Ic Icwork];  % Vector of ave current, upper or lower IGBT.
      Delta_t_Icwork   = t(m) - t(k);  % Switching period for conduction through IGBT.
      Delta_t_Ic           = [Delta_t_Ic Delta_t_Icwork];  % Vector of switching periods.
   else
      Id                   = [Id Icwork];  % Vector of current through diode.
      Delta_t_Idwork   = t(m) - t(k);  % Switching period for conduction through diode.
      Delta_t_Id           = [Delta_t_Id Delta_t_Idwork];  % Vector of diode switching per.
   end
   k      = m;         % Set "k" to most recent value of "m".
   t0     = t(m);      % Set t0
   while (iload(m) > ilower(m)) & (m < length(t))
      m            = m + 1;
      iload(m)  = exp(-R/L*(t(m)-t0))*iload(k) - Vd/R*(1 - exp(-R/L*(t(m)-t0)));
   end
   x = m;
   while (t(m) < t(x) + 3*10^-6) & (m < length(t))
      m            = m+1;
      iload(m)  = exp(-R/L*(t(m)-t0))*iload(k) - Vd/R*(1 - exp(-R/L*(t(m)-t0)));
   end
   Icwork = (iload(k) + iload(m))/2;
   if Icwork < 0
      Ic                   = [Ic Icwork];
```

```
      Delta_t_Icwork  = t(m) - t(k);
      Delta_t_Ic      = [Delta_t_Ic Delta_t_Icwork];
   else
      Id              = [Id Icwork];
      Delta_t_Idwork  = t(m) - t(k);
      Delta_t_Id      = [Delta_t_Id Delta_t_Idwork];
   end
   k          = m;
   delta_t    = t(m) - tswitch;    % Switching period.
   Delta_t    = [Delta_t delta_t];  % Vector of switching periods.
   t0         = t(m);
end

% This next section calculates fmax and fave.
Delta_t             = Delta_t(2:length(Delta_t)-1);  % First and last value are bogus.
max_switching_freq  = 1/min(Delta_t)  % Max.
ave_switching_freq  = length(Delta_t)/Tend  % Average.

% Power Losses
Pc   = 2.5/Tend*sum(abs(Ic.*Delta_t_Ic))   % Conduction.
Psd  = 3.5/Tend*sum(abs(Id.*Delta_t_Id))  % Substrate diode conduction.
if Delta_t_Ic(end) == 0
   Delta_t_Ic(end)    = [];  % Eliminate bogus endpoint.
   Ic(end)            = [];
end
Ps     = .5*Vd*abs((Ic(2:end)./Delta_t_Ic(2:end))*750*10^-9);  % Switching.
Ps     = sum(Ps)/length(Ps)
Prr    = .125 * 19 * 250 * 10^-9 * Vd * max_switching_freq    % Diode reverse recov.
Ptot   = Pc + Psd + Ps + Prr

% Figure(1) is a plot of the load current imposed on the hysteresis band
figure(1);
plot(t,iref,t,iupper,t,ilower,t,iload);
title('Hysteresis Band and Load Current');
xlabel('Time in Seconds');
ylabel('i_r_e_f, Hysteresis Band, and Load Current');

% Figure(2) is a plot of the hysteresis band without the load current
figure(2);
plot(t,iref,t,iupper,t,ilower);
title('Reference Waveform and Hysteresis Band');
xlabel('Time in Seconds');
ylabel('Voltage');

% This section calculates the Fourier series coefficients, plots the first 25,
% and calculates the total harmonic distortion.  It is primarily used for the
```

```
% full power simulation.

% Fourier analysis to determine the THD.  Tech-Note 1702 from MathWorks
% provides guidance on the commands used to extract meaningful information
% using MatLab's fft function.

% First, the fundamental is removed from the load current.
hash = iload - iref;

% MatLab's fft function works fastest at powers of 2.  So, the next highest
% power of 2 that is greater than or equal to length(hash) is calculated.
Nfft            = 2.^(ceil(log(length(hash))/log(2)));
fft_hash        = fft(hash,Nfft);

% fft is symmetric, so throw out the second half
NumUniquePts        = ceil((Nfft+1)/2);
fft_hash            = fft_hash(1:NumUniquePts);

% Find the magnitude of the harmonic components.  Since half were thrown out,
% the value must be multiplied by 2.  This doesn't apply to the dc component
% or the component at the Nyquist frequency.
Mag_fft_hash        = 2*abs(fft_hash);
Mag_fft_hash(1)     = Mag_fft_hash(1)/2;
Mag_fft_hash(end)   = Mag_fft_hash(end)/2;

% Scale the magnitude so it is not a function of the length of hash.
Mag_fft_hash = Mag_fft_hash/length(hash);

% Build the frequency vector to be used in plotting
f = (0:NumUniquePts - 1)*fs/Nfft;
figure(3);
plot(f,Mag_fft_hash);
axis([-1000 max(f)/100 0 max(Mag_fft_hash)]);
title('Frequency Spectrum of Hash');
xlabel('Frequency in Hertz (Hz)');
ylabel('Magnitude');

% This next section computes the frequency spectrum of the load current.
% It is not used to calculate the THD, but is nice to see.

% MatLab's fft function works fastest at powers of 2.  So, the next highest
% power of 2 that is greater than or equal to length(hash) is calculated.
Nfft            = 2.^(ceil(log(length(iload))/log(2)));
fft_iload       = fft(iload,Nfft);

% fft is symmetric, so throw out the second half
```

```
NumUniquePts        = ceil((Nfft+1)/2);
fft_iload           = fft_iload(1:NumUniquePts);

% Find the magnitude of the harmonic components.  Since half were thrown out,
% the value must be multiplied by 2.  This doesn't apply to the dc component
% or the component at the Nyquist frequency.
Mag_fft_iload       = 2*abs(fft_iload);
Mag_fft_iload(1)    = Mag_fft_iload(1)/2;
Mag_fft_iload(end)  = Mag_fft_iload(end)/2;

% Scale the magnitude so it is not a function of the length of hash.
Mag_fft_iload = Mag_fft_iload/length(iload);

% Build the frequency vector to be used in plotting
f = (0:NumUniquePts - 1)*fs/Nfft;
figure(4);
plot(f,Mag_fft_iload);
axis([-1000 max(f)/1000 0 max(Mag_fft_iload)]);
title('Frequency Spectrum of Load Current');
xlabel('Frequency in Hertz (Hz)');
ylabel('Magnitude');

% Compute the THD.
Is1    = A/sqrt(2);  % RMS value of the fundamental
Idis   = sqrt(sum(Mag_fft_hash.^2)/2);  % Distortion
THD    = 100*Idis/Is1
```

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APPENDIX B. MATLAB CODE FOR SIMULATION OF THREE-STATE INVERTER

This code simulates a single-phase hysteresis controlled inverter using the zero voltage state.

```
% Paul F. Fillmore
% Thesis - Hysteresis Band
% This code builds the load current for Zero Voltage State switching.
% The switching scheme is based on a paper written by G. H. Bode and
% D. G. Holmes, "Implementation of three level hysteresis current control
% for a single phase voltage source inverter," 2000 IEEE 31st Annual Power
% Electronics Conference, Vol. 1, pp. 33-38, 2000.
% The object of this program is to calculate acceptable values for
% the hysteresis band, load inductance, and upper and lower rail voltage.
% A plot of the load current, reference waveform, and hysteresis band is
% generated in addition to calculating the maximum switching frequency.

h        = .75;  % hysteresis band
Vd       = 375;   % rail voltage should be interpreted as +Vd and - Vd.
R        = 2.7;    % load resistance
L        = .002125;  % load inductance
A        = 92;      % amplitude of reference
fs       = 60*200000;   % Sampling frequency
fn       = fs/2;       % Nyquist frequency (used for fft)
Tend     = 1/60;       % time period
t        = 0:1/fs:Tend;
iref     = A*sin(2*pi*60*t);  % reference sine wave
iupper   = iref + h;          % upper hysteresis band
iupper2= iupper + .7*h;
ilower   = iref - h;          % lower hysteresis band
ilower2= ilower - .7*h;

t0       = 0;
ts       = t0;
iload    = zeros(size(iref));
Delta_t = 0;
m        = 1;
k        = m;
trigger = 0;
delay    = 0;
exit     = 0;
Ic       = 0;
Id       = 0;
Delta_t_Ic = 0;
```

```
Delta_t_Id = 0;
while (t0 < t(length(t)) & exit <= length(t) + 5000)
   exit = exit + 1;
   while ((trigger == 0) & (m < length(t)))
      m          = m + 1;
      iload(m)  = exp(-R/L*(t(m)-t0))*iload(k) + Vd/R*(1 - exp(-R/L*(t(m)-t0)));
      if iload(m) > iupper(m)
         trigger = 1;
         x        = m;  % Control index to establish 3microsecond delay
         while (t(m) < t(x) + 3*10^-6) & (m < length(t)) & (delay == 0)
            m             = m+1;
            iload(m)      = exp(-R/L*(t(m)-t0))*iload(k) + Vd/R*(1 - exp(-R/L*(t(m)-t0)));
         end
         Iwork = (iload(m) - iload(find(t == t0)))/2;
         if Iwork >= 0
            Ic             = [Ic Iwork];
            Delta_t_Ic   = [Delta_t_Ic t(m)-t0];
         end
         if Iwork < 0
            Id             = [Id Iwork];
            Delta_t_Id   = [Delta_t_Id t(m)-t0];
         end
      end
   end

   t0 = t(m);
   k  = m;
   while ((trigger == 1) & (m < length(t)))
      m          = m + 1;
      iload(m)  = exp(-R/L*(t(m)-t0))*iload(k);
      if iload(m) > iupper2(m)
         trigger = 2;
         x        = m;  % Control index to establish 3microsecond delay
         while (t(m) < t(x) + 3*10^-6) & (m < length(t))
            m             = m+1;
            iload(m)      = exp(-R/L*(t(m)-t0))*iload(k);
         end
         Iwork          = (iload(m) - iload(find(t == t0)))/2;
         Id             = [Id Iwork];
         Delta_t_Id     = [Delta_t_Id t(m)-t0];
      end
      if iload(m) < ilower(m)
         trigger = 3;
         x        = m;  % Control index to establish 3microsecond delay
         while (t(m) < t(x) + 3*10^-6) & (m < length(t))
            m             = m+1;
```

```
        iload(m)      = exp(-R/L*(t(m)-t0))*iload(k);
      end
      Iwork           = (iload(m) - iload(find(t == t0)))/2;
      Id              = [Id Iwork];
      Delta_t_Id      = [Delta_t_Id t(m)-t0];
   end
end
t0 = t(m);
k  = m;
while ((trigger == 2) & (m < length(t)))
   m          = m + 1;
   iload(m)  = exp(-R/L*(t(m)-t0))*iload(k) - Vd/R*(1 - exp(-R/L*(t(m)-t0)));
   if iload(m) < ilower(m)
      trigger = 3;
      x       = m;  % Control index to establish 3microsecond delay
      while (t(m) < t(x) + 3*10^-6) & (m < length(t))
         m            = m+1;
         iload(m)     = exp(-R/L*(t(m)-t0))*iload(k) - Vd/R*(1 - exp(-R/L*(t(m)-t0)));
      end
      Iwork = (iload(m) - iload(find(t == t0)))/2;
      if Iwork >= 0
         Ic           = [Ic Iwork];
         Delta_t_Ic   = [Delta_t_Ic t(m)-t0];
      end
      if Iwork < 0
         Id           = [Id Iwork];
         Delta_t_Id   = [Delta_t_Id t(m)-t0];
      end
   end
end
t0 = t(m);
k  = m;
while ((trigger == 3) & (m < length(t)))
   m          = m + 1;
   iload(m)  = exp(-R/L*(t(m)-t0))*iload(k);
   if iload(m) < ilower2(m)
      trigger = 4;
      x       = m;  % Control index to establish 3microsecond delay
      while (t(m) < t(x) + 3*10^-6) & (m < length(t))
         m            = m+1;
         iload(m)     = exp(-R/L*(t(m)-t0))*iload(k);
      end
      Iwork           = (iload(m) - iload(find(t == t0)))/2;
      Id              = [Id Iwork];
      Delta_t_Id      = [Delta_t_Id t(m)-t0];
   end
```

```
      if iload(m) > iupper(m)
         trigger = 1;
         x       = m;  % Control index to establish 3microsecond delay
         while (t(m) < t(x) + 3*10^-6) & (m < length(t))
            m            = m+1;
            iload(m)     = exp(-R/L*(t(m)-t0))*iload(k);
         end
         Iwork           = (iload(m) - iload(find(t == t0)))/2;
         Id              = [Id Iwork];
         Delta_t_Id      = [Delta_t_Id t(m)-t0];
      end
   end
   t0 = t(m);
   k  = m;
   if trigger == 4
      delta_t    = t0 - ts;
      Delta_t    = [Delta_t delta_t];
      ts         = t0;
   end
   while ((trigger == 4) & (m < length(t)))
      m          = m + 1;
      iload(m)  = exp(-R/L*(t(m)-t0))*iload(k) + Vd/R*(1 - exp(-R/L*(t(m)-t0)));
      if iload(m) > iupper(m)
         trigger = 1;
         x       = m;  % Control index to establish 3microsecond delay
         while (t(m) < t(x) + 3*10^-6) & (m < length(t))
            m            = m+1;
            iload(m)     = exp(-R/L*(t(m)-t0))*iload(k) + Vd/R*(1 - exp(-R/L*(t(m)-t0)));
         end
         Iwork = (iload(m) - iload(find(t == t0)))/2;
         if Iwork >= 0
            Ic           = [Ic Iwork];
            Delta_t_Ic   = [Delta_t_Ic t(m)-t0];
         end
         if Iwork < 0
            Id           = [Id Iwork];
            Delta_t_Id   = [Delta_t_Id t(m)-t0];
         end
      end
   end
end
Delta_t                  = Delta_t(2:length(Delta_t)-1);
max_switching_freq   = 1/min(Delta_t)  % max switching frequency
%ave_switching_freq = 1/mean(Delta_t)
ave_switching_freq2  = (length(Delta_t))/Tend
```

```
Pc      = 2.5/Tend*sum(abs(Ic(2:end).*Delta_t_Ic(2:end)))   % Conduction
Psd     = 3.5/Tend*sum(abs(Id(2:end).*Delta_t_Id(2:end)))  % Substrate diode cond
Ps      = Vd*abs((Ic(2:end)./Delta_t_Ic(2:end))*750*10^-9);  % Switching
Ps      = sum(Ps)/length(Ps)
Prr     = .125 * 19 * 250 * 10^-9 * Vd * max_switching_freq   % Diode reverse recovery
Ptot    = Pc + Psd + Ps + Prr

figure(1);
plot(t,iref,t,iupper,t,ilower,t,iload);
title('Hysteresis Band and Load Current');
xlabel('Time in Seconds');
ylabel('i_r_e_f, Hysteresis Band, and Load Current');
```

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APPENDIX C. WIRING AND PIN DIAGRAMS

This appendix serves as a reference for follow-on work. The wiring and pin diagrams will assist in further testing of the existing inverter or building additional units.

A. THE CONTROLLER

Figure 30 shows the actual controller. Labels A, B, C, and D identify the corresponding pin diagrams in Figures 31 and 32. Label A is the ±15 V connection for the Hall effect devices. Label B is the connection for input and output control signals. Label C is the control circuitry for phase c. (Phases a, b, and c utilize identical control circuitry.) Label D is the power supply connection for the controller. Controller power is supplied from two dc–dc converters underneath the controller board.

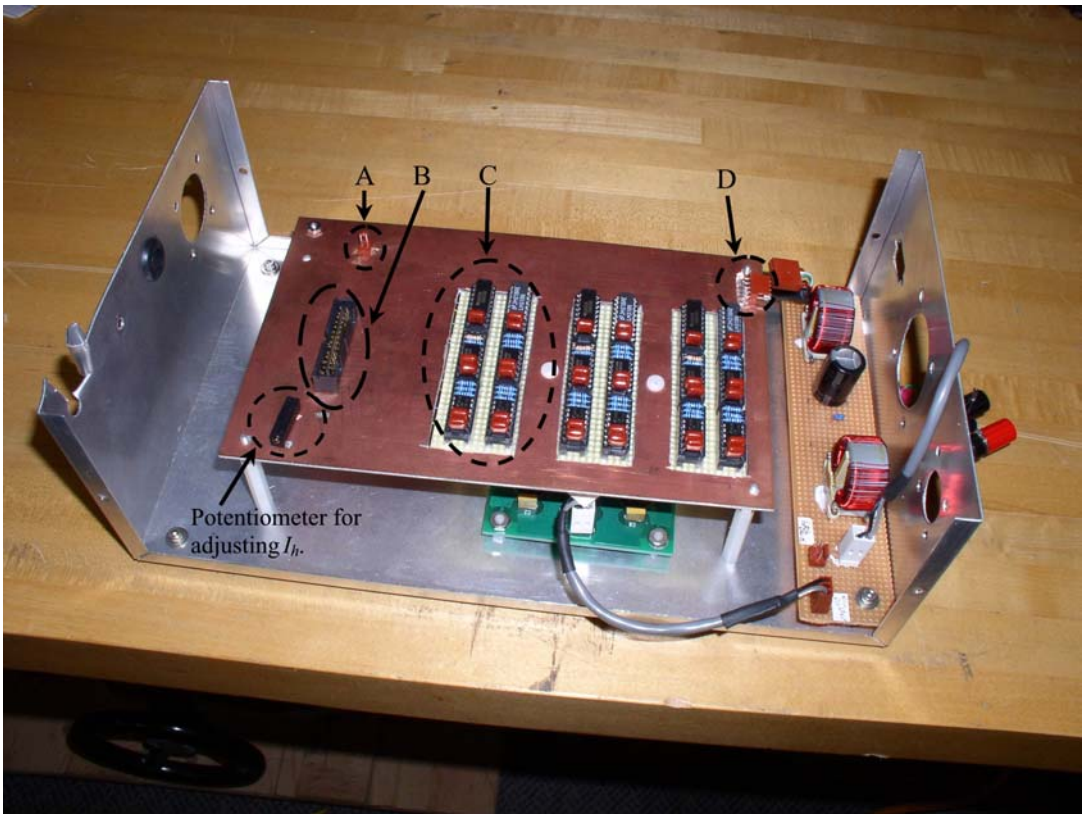

Figure 30. Controller.

Label A Wiring Diagram

Pin #	1	2
Value	15 V	–15 V

Label B Wiring Diagram

Connection	Pin #		Connection
i_{out_c}	2	1	GND
$i_{ref\_c}–I_h$	4	3	GND
i_{ref_c}	6	5	GND
$i_{ref\_c}+I_h$	8	7	GND
i_{out_b}	10	9	GND
$i_{ref\_b}–I_h$	12	11	GND
i_{ref_b}	14	13	GND
NC	16	15	GND
$i_{ref\_b}+I_h$	18	17	GND
i_{out_a}	20	19	GND
$i_{ref\_a}–I_h$	22	21	GND
i_{ref_a}	24	23	GND
$i_{ref\_a}+I_h$	26	25	GND

Figure 31. Wiring Diagrams for Labels A and B of Figure 33.

Label C Wiring Diagram

Row #	Column A	Column B	Column C	Column D
1	6A	GND	6C	GND
2	4B	GND	4D	GND
3	*LM741*		*LM741*	
4		15 V		15 V
5	i_{ref}	4A	I_h	4C
6	–15 V		–15 V	
7	5B		5D	13C
8	7B	5D	14C	GND
9	5B	14C	13C	14D
10	15A	GND	15C	GND
11	13B	GND	13D	GND
12	*LM318*		*LM318*	
13		15 V		15 V
14	7B			
15	–15 V		–15 V	
16	13A	14B	23B	5 V
17	13A	GND	25A	i_{out}
18	27A	5 V		
19	26A	GND	21D	GND
20	24B	GND		
21	*LM319*			15 V
22			24C	GND
23	GND	26C	25C	GND
24	14D	15 V	*CD4001*	
25	26B	14B		
26	–15 V			GND
27	21C	GND		GND

Label C Part Placement

Row #	Column A	Column B	Column C	Column D
1	0.1 µF		0.1 µF	
2	0.1 µF		0.1 µF	
3	*LM741*		*LM741*	
4				
5				
6				
7	10 kΩ		10 kΩ	
8	10 kΩ		10 kΩ	
9	10 kΩ		10 kΩ	
10	0.1 µF		0.1 µF	
11	0.1 µF		0.1 µF	
12	*LM318*		*LM318*	
13				
14				
15				
16	10 kΩ		10 kΩ	
17	10 kΩ		100 Ω	
18	10 kΩ			
19	0.1 µF		0.1 µF	
20	0.1 µF			
21	*LM319*		*CD4001*	
22				
23				
24				
25				
26				
27				

Label D Wiring Diagram

Connection	Pin #
5 V	1
GND	2
GND	3
15 V	4
–15 V	5

Figure 32. Wiring Diagrams for Labels C and D of Figure 33.

B. IGBT DRIVERS

Figure 33 is a picture of three IGBT drivers mounted on a circuit board. Each driver provides the gating for one IGBT module (a half-bridge). The circuit board has its own dc–dc converter to power the drivers. In order to disable the V_{ce} monitoring, two of the terminals must be shorted and Figure 33 shows an example of how this is accomplished using yellow wire-wrap wire. Figure 34 is the schematic for the circuit board.

Figure 33. IGBT Drivers.

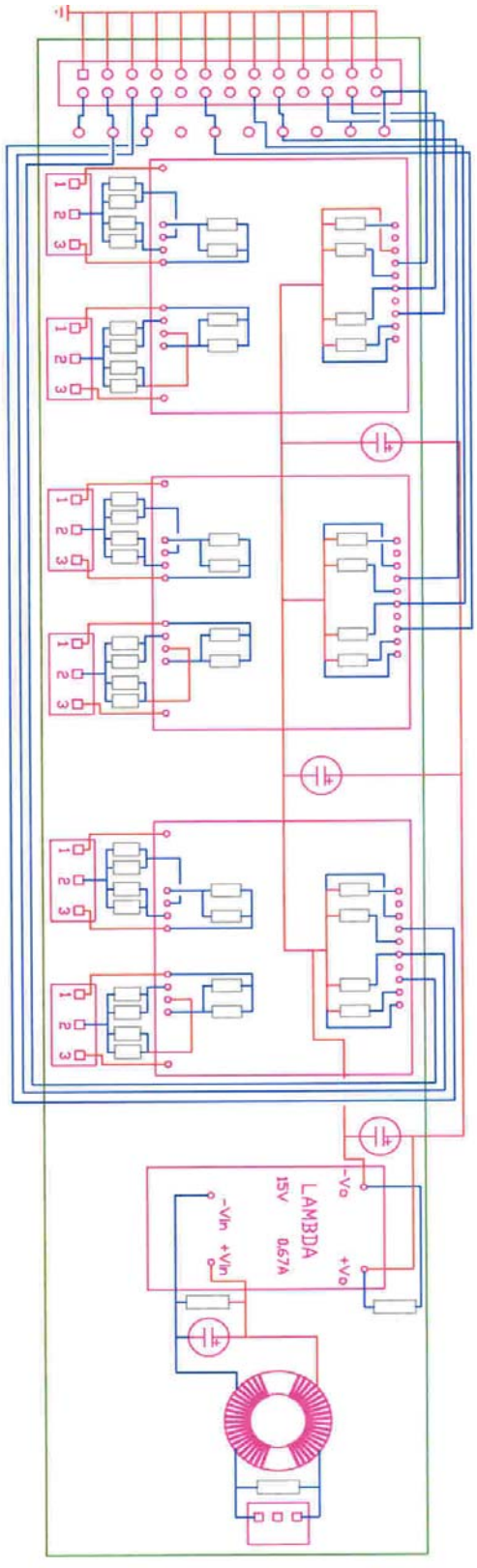

Figure 34. IGBT Drivers Circuit Board Schematic.

C. HALL EFFECT DEVICES

The Hall effect devices are mounted on their own circuit board and are shown along side the IGBTs in Figure 10. Figure 35 is the schematic for the circuit board.

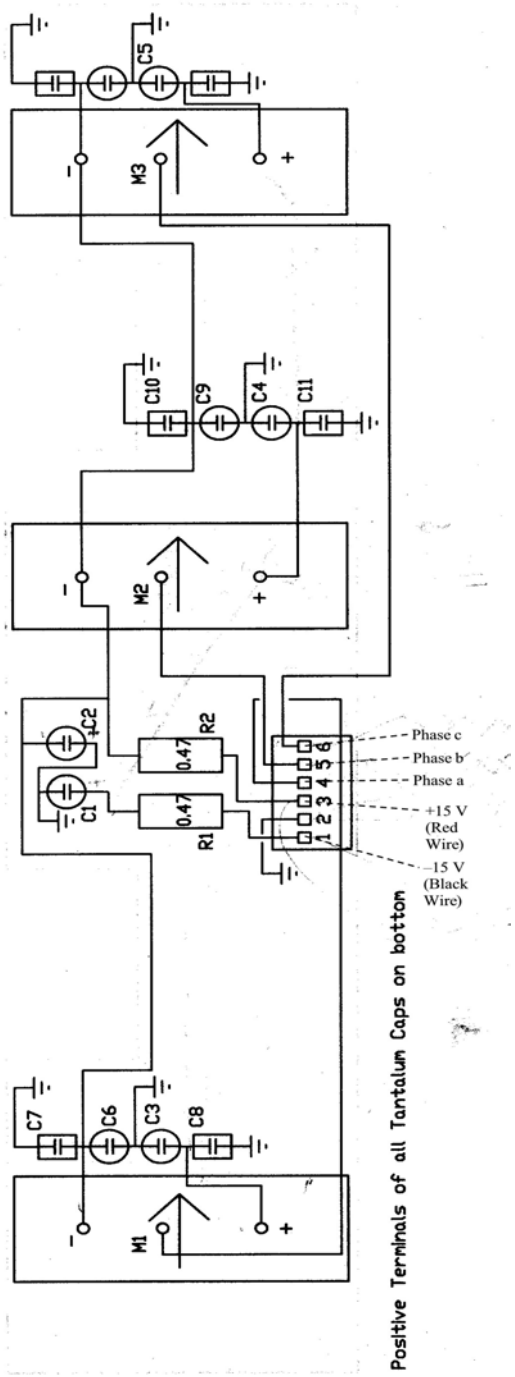

Figure 35. Hall Effect Devices Circuit Board Schematic.

D. DC–DC CONVERTERS

Two dc–dc converters are used to power the control circuitry, one to provide ±15 V (Power-One® DFC10U24D5) and the other to provide 5 V (Power-One® DFA6U12S15). They are mounted on a single circuit board underneath the controller. Figure 36 is the schematic for the circuit board.

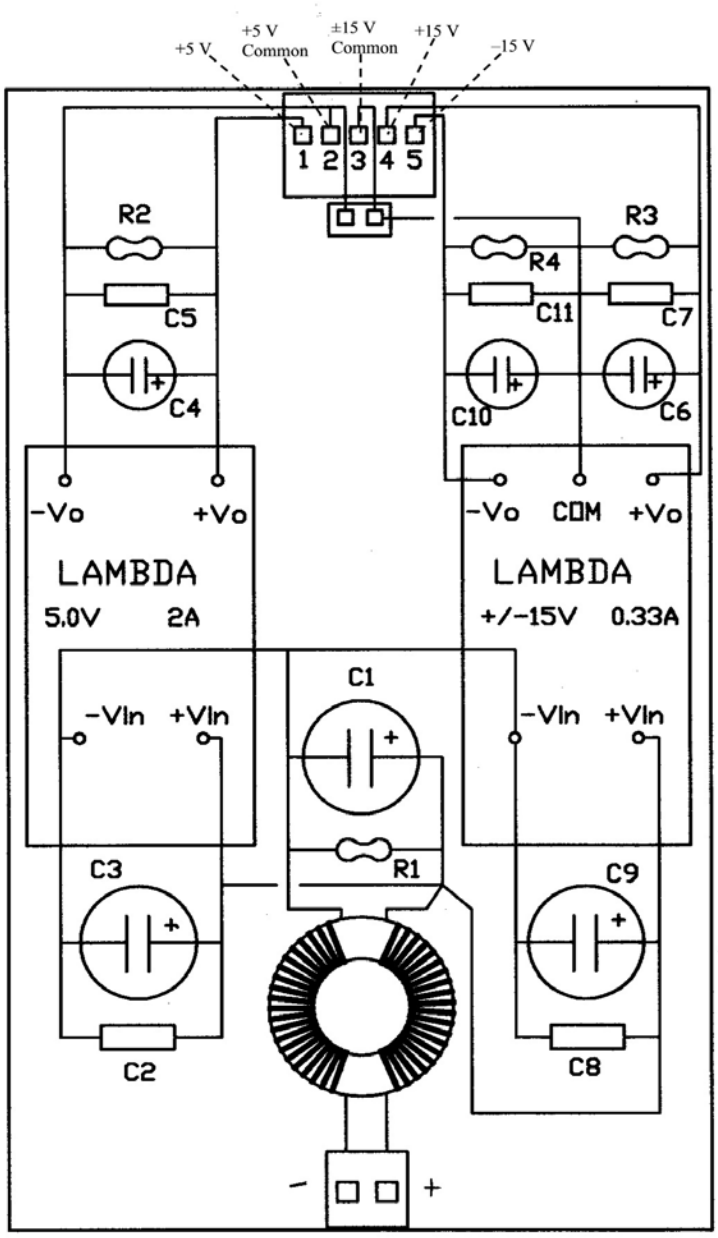

Figure 36. DC–DC Converters Circuit Board Schematic.

E. HYSTERESIS CIRCUIT FROM UNIVERSITY OF MISSOURI-ROLLA

The original hysteresis control circuit proposed by University of Missouri-Rolla is shown in Figure 37. The schematic was modified to meet the needs of this thesis.

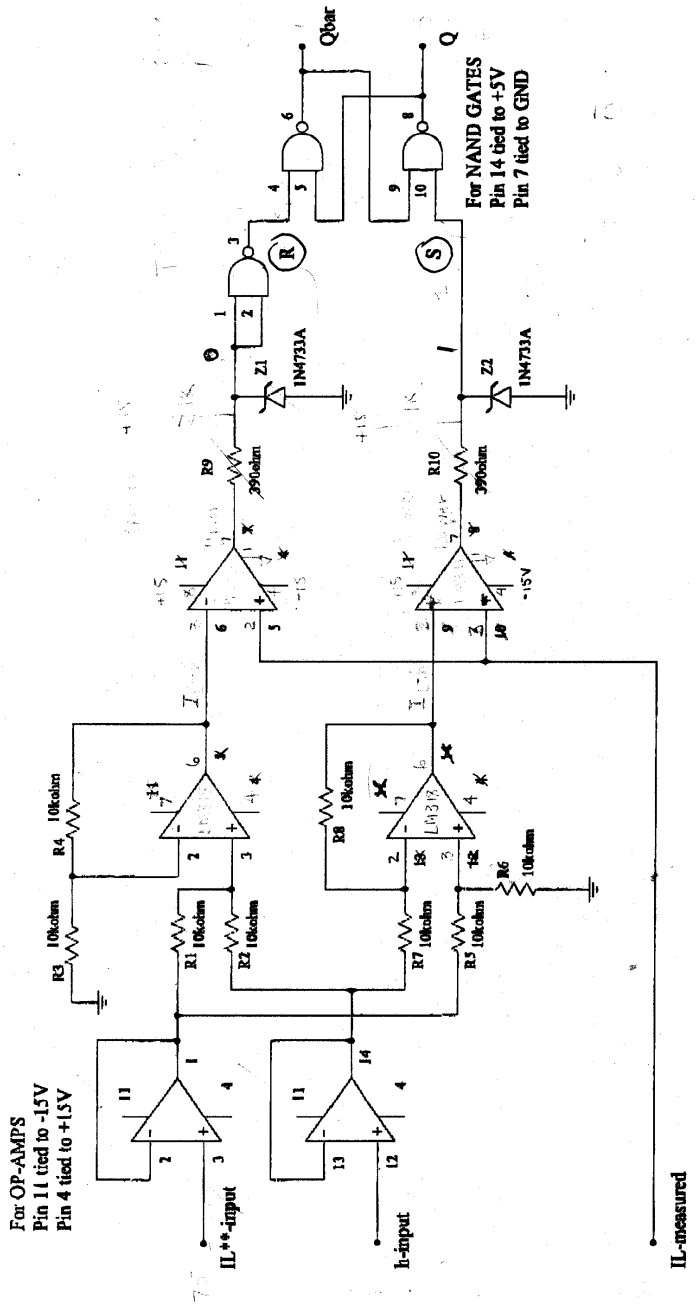

Figure 37. University of Missouri-Rolla Hysteresis Control Circuit Diagram [From Ref. 11.].

F. WIRING DIAGRAM FOR THREE-PHASE REFERENCE

The three-phase reference signal was generated using Programmable Logic Devices (PLD). Figure 38 shows the basic circuit for a single phase. Each other phase is identical, but with a 120 degree phase shift from the others. All three phases are fed from the same oscillator chip. Since the PLDs output a 36-step sine wave, the clock signal is 2.16 kHz to output a 60 Hz signal ($36 \times 60 = 2160$). Capacitor C1 (1.5 µF) provides the necessary filtering to smooth the resistor tree output into a sinusoidal waveform.

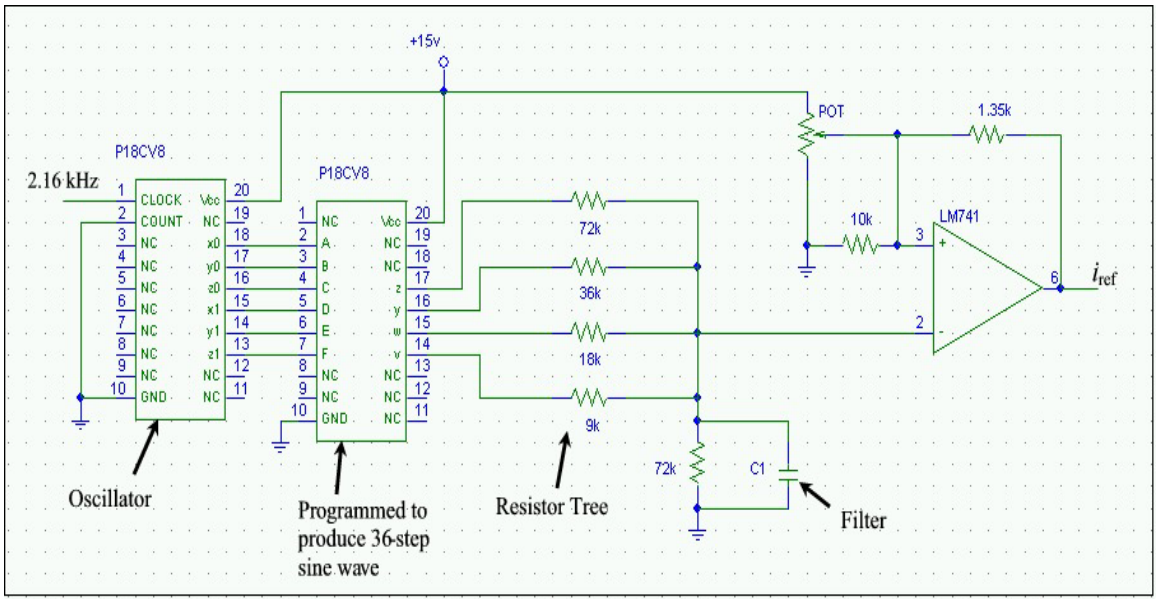

Figure 38. Sine Wave Generating Circuit.

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